Characterization and modeling of static properties and low-frequency noise in organic field-effect transistors (OFETs)

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Caractérisation et modélisation des propretés électriques et du bruit à basse fréquence dans les transistors organiques à effet de champ (OFETs)

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Characterization and modeling of static properties and low-frequency noise in organic field-effect transistors (OFETs)

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Ph.D thesis prepared at IMEP-LAHC laboratory, INP-Grenoble, France
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Contents

Introduction

Since 1960s, the modern industry of microelectronics began to utilize the crystalline materials of simple elements, e.g. Si and Ge, or some compounds, e.g. InSb and GaAs, to make the basic devices for the integrated circuits(ICs). Till now, the Si-based technologies and devices are still the main stream. However, with the challenges arising from the considerable miniaturization, further development becomes more and more severe. On the other hand, many new materials and new technologies are emerging, such as nano wire, graphene and organic materials (OMs).

In fact, the OMs have been studied from 1940s, but due to their poor electrical characteristics (high resistivity, low mobility) and the lack of understanding of transport mechanism during that time, the progress in this domain remained relatively very slow. This situation lasted till 1986, the first appearance of organic transistor.[4] It was made with a thin film of polythiophene obtained by an electrochemical process. Such a demonstration reveals the feasibility to fabricate organic transistors, and immediately attracted much interest from the areas of industry and academic research.

The principal advantages of organic electronics are:

- **Large area:** The conventional technologies of semiconductors are limited by the wafer size, e.g. 300mm, the maximum of the actual single-crystal silicon technology. It is difficult to apply for the circuits of large surface, such as flat-panel display. However, the organic transistors could be fabricated on the large substrate of plastic film, even paper,[6] by the methods such as printing. They are naturally suitable for the large area applications.
- **Structural flexibility:** Because of the weak van der Waals force interacting between organic molecules, the OMs exhibit good mechanic characteristics, especially polymer, and moreover, the organic transistors using amorphous or polycrystalline OMs could be made on the flexible substrates. The circuits based on such OFETs will be very appropriate for the flexible applications such as surface strain sensors. In addition, this flexibility will also improve the portability and the robustness. For instance, we could envisage the electronic products that could be rolled up or folded to carry without worry of damage.
- **Low temperature fabrication:** The conventional Si technologies usually use very high temperature to prepare the single-crystal wafer, to deposit or evaporate the contact/interconnection metals and to oxidize the silicon to form the SiO_2 dielectric or passivation layer. Even the minimum temperature for the deposition of amorphous silicon on the glass substrate, a standard process to fabricate the flat-panel display, it still attains to 360ºC. Such high temperatures obviously cannot be used for plastic or paper substrates, but the organic materials could be prepared and deposited at even room temperature (RT) because of the weak van der Waals forces bonding in the OMs.
- **Wide range of functionalities:** The organic chemistry enables us to synthesize the materials with various functionalities to adapt to different applications: e.g. solubility, energy level, band-gap, structural properties and doping. Therefore, there are some demonstrations of the hybrid organic-inorganic materials that take advantages of the special properties of both kinds of semiconductors, e.g. the superior carrier mobility of inorganic semiconductors and the processability of organic materials.[7]
- **Low cost:** The high temperatures for conventional technologies require complicated equipments and consume a lot of energy. However, for the organic transistors, the processes are much simpler. For example, the mass-produced roll-to-roll printing technology at RT will bring very low cost. Certainly, less chemical products and less metal are used in the manufacture, which will decrease the influence on the natural environment and thus decrease the cost to treat them.

The main applications of organic devices are mentioned below:

■ **Large-scale integrated circuits:** The limitation of wafer size in conventional silicon-based technologies is no longer a problem for organic electronics, because organic integrated circuits (ICs) can be fabricated on a substrate of very large surface, e.g. roll-to-roll printing on a flexible plastic substrate. This special feature enables many applications, e.g. large-surface sensor, flat-panel display, surface lighting, photovoltaic, where the silicon ICs is not appropriate due to either high cost or processing difficulties.

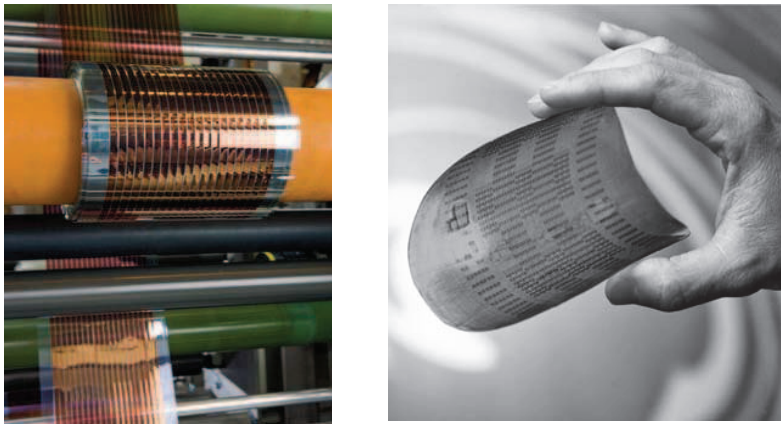

Figure I-1 | Left: Roll-to-roll production of flexible organic photovoltaic modules. (After OE-A brochure, 3rd Edition, 2009) Right: Fully processed 150nm wafer foil containing all-polymer transistors and integrated circuits. (After ref.,[2] P332)

■ **Flat-panel display:** The switching devices for the present active matrix flat-panel display (AMFPD) are generally based on the amorphous silicon. The size of glass substrate limits the cost reduction, however, the nearly non size-limited substrate for the OFETs' fabrication could enable very large displays, based on either liquid crystal pixels or organic light-emitting diode(OLED). The SONY OLED television has been released into the commercial market, the future OLED TV will be fully organic, very light weight, flexible and transparent, of course, with very high image quality.

Figure I-2 | Left: The first reported active-matrix display with organic semiconductors. The display contains 64 pixels and is driven by 4096 polymer TFT, with solution processed PTV as the active semiconductor. An image containing 256 gray levels is shown and the display is refreshed at 50Hz. (After ref.,[2] P347) Right: Full-HD OLED TV with thickness as small as 1cm.

■ **Sensor and scanner:** The large surface and flexibility are very suitable for the surface strain sensor which has been applied to simulate the human skin.[8] At the same time, those properties could be used to make the scanner that scans the image from rough and large surface at only one time, instead of the conventional sweeping mode.

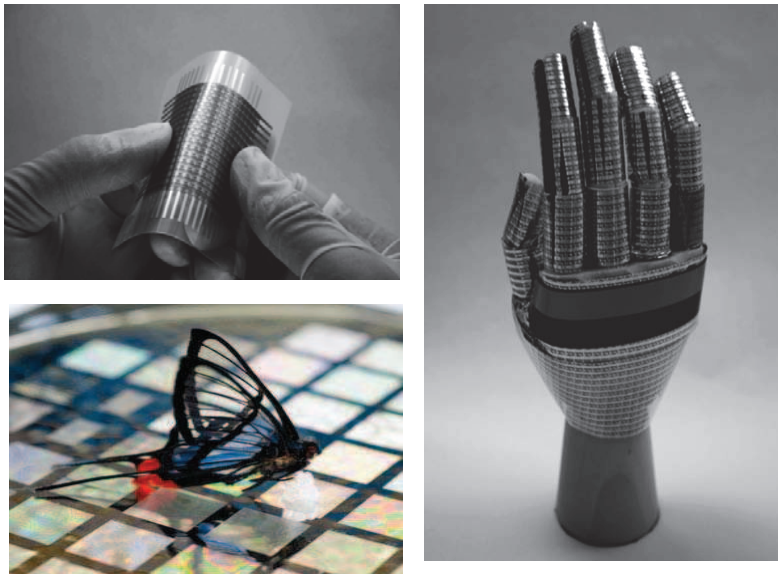

Figure I-3 | Upper-left: A flexible, large-area pressure sensor. Organic transistors active matrix is formed on a plastic film and integrated with pressure-sensitive rubber. (After ref.,[1] P530) Lower-left: Very high sensitivity pressure sensor developed by Bao group at Stanford University.[5] Such an array of high sensitivity sensors can feel the slight touch by butterfly. Right: An image of electronic artificial skin attached on the robot surface. A plastic film with organic transistors, a pressure-sensitive rubber sheet, and a plastic film with top electrode are laminated together to form a large-area pressure sensor. (After ref.[1], P531)

■ **RFID tags:** The organic RFID tags have shown much greater advantages compared to the currently used code bar for the domains of retail and logistics because of their very low cost, flexibility, good robustness.[9] For example, the application to the red wine, the organic RFID tags offer much more information, such as the brand history, planting environments, fermenting methods, recommendations of conservation and drinking. For more details on organic RFID tags can refer to ref.,[1] chapter 6.1.

Figure I-4 | Left: Printed RFID tags. (After OE-A brochure, 3rd Edition, 2009) Right: RFID tags for brand protection. (After OE-A brochure, 2nd Edition, 2007)

■ **Lighting:** Electroluminescent (EL) and OLED lighting are of great potential for novel large-area, energy-efficient, low-cost but high quality solid-state lighting and decoration solution. OLED has been widely applied for displays as backlighting or active cells. The first OLED designer lamps are already available in the commercial market and it will quickly be moved for further applications with improvements made in efficiency, color purity, lift time and manufacturing.

Figure I-5 | Left: OSRAM OLED designer lamp. (After OE-A brochure, 3rd Edition, 2009) Right: New OSRAM OLED lighting, from spotlights to walls of light. (After OE-A website)

■ **Solar cells:** The present solar cells are generally based on the polycrystalline silicon. Their high price obstructs the large-scale application. However, the much lower-cost and the flexibility of organic transistors will offer an ideal photovoltaic solution that could be installed everywhere. Their less environmental pollution is also consistent with the future conception of green energy.

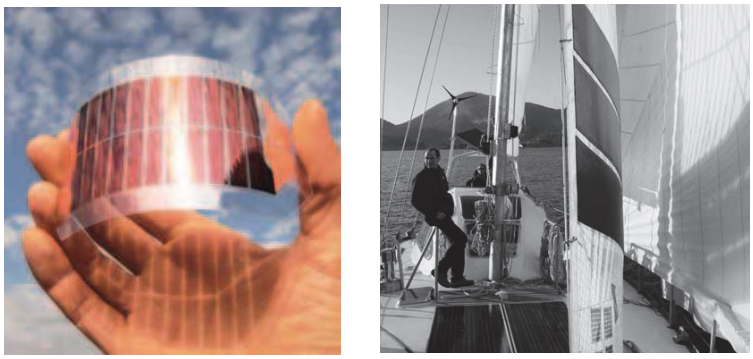

Figure I-6 | Left: Flexible organic photovoltaic cell. (After OE-A brochure, 3rd Edition, 2009) Right: The ship currently navigates in Italian sea using a hybrid motor (diesel + electric) with solar electricity being produced by either Si or organic (polymer with carbon nanotubes) photovoltaic thin films. (After book "*Flexible Solar Cells*",[3] P105)

Despite so many encouraging advantages and applications, there are a lot of issues remained on organic materials and organic transistors. For instance, very low performances, rapid degradation and thus short life time. All these drawbacks destine that the organic transistors can only be applied for the low frequency or low performance purposes. At this stage, they cannot rival their conventional counterpart: silicon.

Upon these observations, we will address in this thesis some main issues in five chapters:

1. **Organic materials**. The carrier transport in organic semiconductors in comparison with that in single-crystal silicon will be firstly presented. Next, one deals with the principal parameters and then the typical organic semiconductors: small molecular, polymeric and n-type semiconductors etc. In the end, the other (organic) materials used for OFETs' fabrication are also analyzed: including organic dielectrics, organic electrodes and interconnections, organic substrates as well as organic passivation layers
2. **Organic field-effect transistors (OFETs)**. The OFETs' structures and their impacts on electrical properties as well as the operating mechanism are first presented. And then, we study the OFETs' principle parameters: mobility, threshold voltage, contact resistance, subthreshold slope etc. The relevant issues and critical results in the literature are also addressed. Finally, we investigate the principal techniques for organic transistors fabrication.
3. **Static electrical characterization of organic transistors**. The mostly used method in the community is firstly discussed and then we introduce our Y function method. Afterwards, one addresses other methods in the literature for the principal parameters extraction, including our modified and power TLM. In the end, we present the principal results of our studied OFETs in this thesis.
4. **Modeling**. A modeling on the OFETs' DC characteristics is first presented where a 1-D Poisson equation solution is provided. Next, the attention is paid to the carrier transport in organic semiconductors on the basis of the experimental data (low temperature measurements) obtained in a set of TIPS-pentacene OFETs. Afterwards, we theoretically analyze the carrier mobility in organic transistors.
5. **Low-frequency noise**. First, the basic noise theory and the analysis methods are presented. And then, we analyze the low-frequency noise in pentacene OFETs where a clear domination of contact noise is observed. Next, we propose a contact noise extraction method by extending the DC TLM to noise analysis. This method is successfully applied into our two sets of OFETs. With the extracted contact noise, we develop a diagnostic process

for the contact noise in staggered OFETs. In the end, the results obtained on different OFETs are also described as well.

Each chapter will briefly introduce the basic theories of classical silicon and the silicon based MOSFETs, since the literature showed that most of the theories for Si MOSFETs are also applicable to the organic transistors. A discussion started with comparison is also easier for understanding.

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Chapter 1
Organic semiconductors

The earliest organic semiconductors were generally used for the optical devices, and this situation lasted from 1940s till now. The recent progresses made in the material engineering and fabrication technologies permit to improve the carrier transport properties in the organic devices, such as organic light-emitting diode (OLED), organic solar cells and organic field-effect transistors (OFETs).

For a better understanding, it is useful to briefly compare the transport properties of organic semiconductors with the classical inorganic semiconductors, such as silicon (Si).

1.1 CARRIER TRANSPORT MECHANISM

■ Silicon

In the silicon crystal, every atom (valence IV) is strongly linked to the four neighboring atoms by the covalent bonds. The binding energies are as high as 76kcal/mol,[3] which is much higher than the lattice vibrational energy, the lattice arrangement is thus not significantly affected by the phonons. Hence the lattice periodicity is nearly kept perfect, and the crystal is called rigid. In this kind of medium, the charge carriers could move as highly delocalized plan waves (Bloch waves) with very high velocity. However, due to the presence of diffusion centers (e.g., phonons or defects), the charge carriers cannot always accelerate under an electrical field but rather have a mean free path, in which they move without interaction. Note that the kinetic energy of carriers is obtained from two collisions, exhibiting a mean drift velocity which decreases with the temperature since the number of phonons increases at higher temperatures. Therefore, the mean velocity obtained by unit electrical field is defined as mobility, μ (cm^2/Vs). In silicon, the values of μ at room temperature can attain 1400 cm^2/Vs and 500 cm^2/Vs, for the electrons and the holes, respectively.

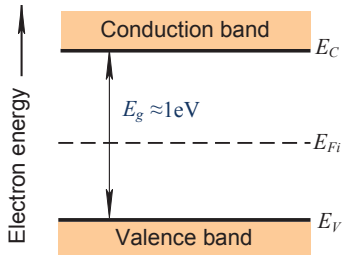

Figure 1.1 | Band diagram of non-doped single-crystal silicon solid, where the Fermi level resides at its intrinsic level, i.e., in the middle of band-gap. The band-gap energy is around 1eV.

The conducting type of silicon semiconductor depends on the majority impurities that are often called dopant. The dopant changes the thermal equilibrium of intrinsic semiconductors to conduct principally by one type of carriers: either electrons or holes. Hence there are two types of doping: if the dopant introduces excess electrons into the silicon, it is referred as to donor (valence V), on the other hand if the dopant introduces excess holes, it is referred as to acceptor (valence III). So, we have two kinds of classical semiconductors: p-type and n-type.

■ Organic semiconductors

In the organic semiconductors, the molecules are bonded together by very weak van der Waals forces whose energy is small than 10kcal/mol.[3] This energy is comparable to that of phonons at

room temperature. For this reason, the lattice cannot be regarded as rigid as in the single-crystal silicon. The loss of periodicity obviously results in a loss of carrier delocalization, and consequently the mobility is very small, typically less than 10 cm^2/Vs. Due to the weak interaction among the molecules, the band thickness is very narrow, as small as 0.1eV(1% of that of Si).[5] In general, the narrow bands will also lead to small carrier mobility. Hence for the organic semiconductors, the conventional conduction band and valence band are replaced by the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), respectively.

In the work of Ishii *et al.*,[2] they explicitly discuss the formation of LUMO and HOMO in the organic semiconductors. Fig. 1.2a shows the electronic structure of a hydrogen atom, where the potential well is the Coulombic potential resulted from the atomic nucleus. Various atomic orbitals (AOs) are formed in this well, and an electron occupies the lowest 1s orbital. The upper limit is the vacuum level (*VL*), above which the electron can escape from the atom. The definition of *VL* will be discussed in detail in the next chapter, for the interface dipole. Fig. 1.2b shows a polyatomic molecule or a single polymer chain, the effective well of an electron is created by the atomic nuclei and other electrons. The wells of the nuclei are merged in the upper part to shape up a broad well. Deep AOs are still localized in the atomic potential well (core levels), but the upper AOs interact to form delocalized molecular orbitals (MOs). The outermost horizontal limit of the potential well is always the *VL*. The energy differences from the highest occupied MO (HOMO) or lowest unoccupied MO (LUMO) to the *VL* are the ***gas phase*** ionization energy I_g or the electron affinity χ_g of the molecule, respectively. As individual molecules or polymer chains approach to form solid, the electronic structure becomes like shown in Fig. 1.2c. Since the molecules interact by the weak van der Waals forces, the top part of the occupied valence states (or valence band) and the lower unoccupied states (conduction band) are usually localized in each molecule, with very narrow intermolecular band widths of <0.1eV. Therefore, the OSC electronic structure remains that within its original molecule or single chain, and the application of the conventional band theory (assuming itinerant electrons) is limited. The highest occupied state and the lowest unoccupied state are denoted as HOMO and LUMO, respectively.

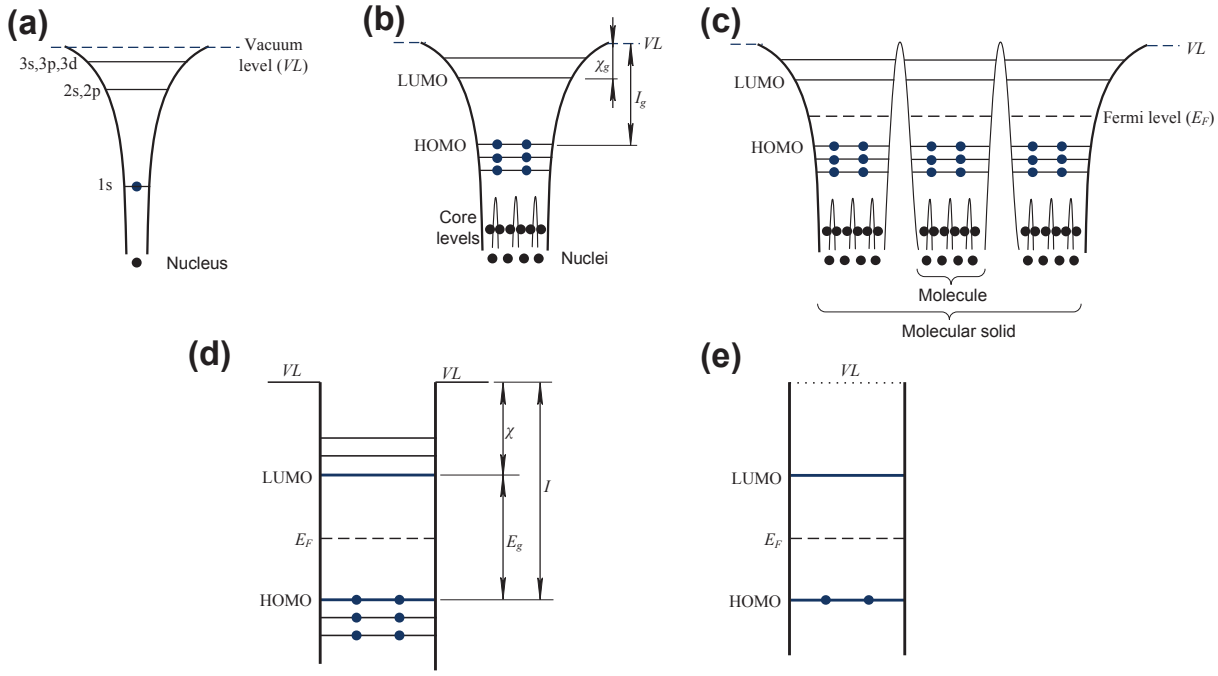

Figure 1.2 | Electronic structure represented with potential wells. (a) Hydrogen atom (b) Polyatomic molecule (c) Organic solid (d) and (e) simplification of (c). (remade but after Ishii 1999[2])

The electronic structure in Fig.1.2c is sometimes simplified as shown in Figs. 1.2d and 1.2e. The Fermi energy is denoted as E_F and because the electron distribution obeys the Fermi statistics, the definition of Fermi level can be also applied. The ionization energy I and electron affinity χ of the organic semiconductor are also defined as the energy difference of the HOMO and the LUMO from the *VL*, respectively, alike in molecule. Note that the values of I and χ might be different from those for an isolated molecule (I_g, χ_g) because of multielectronic effect. This is due to the fact that in condensed state, the electronic polarization in molecules surrounding the ionized molecule stabilizes the ion (polarization energies P_+ and P_- for the hole and the electron, respectively), lowering the ionization energy and increasing the electron affinity from those in gas phase. The OSC work function Φ is similarly defined as the energy difference from the Fermi level to the *VL*.

Up to now, an explicit picture of the carrier transport mechanisms in organic semiconductors is still lacking. This is because the mixture of different materials, different crystalline structures and different manufacturing methods, which leads to the complex mixture of various transports. Nevertheless at present, there are several principal transport mechanisms in the literature which can account for the carrier transport in most of organic semiconductors.

1. **Band-like transport:** In organic semiconductors, the mean free paths of carriers are often comparable or less than the intermolecular spacing,[6] the band-like transport is not believed to be a major transport mechanism. This is reasonable since in the disordered system, the transport may be dominated by the hopping, as discussed later. However in the highly pure single-crystal organic materials, such as rubrene[7] and TIPS-pentacene,[8, 9] the recent works found that the carrier mobility is quite high, greater than 10 cm^2/Vs and more importantly, the temperature dependence of mobility shows a negative dependence $d\mu/dT<0$ and the mobility exhibits a clear isotropy in Hall Effect measurement,[7] all of which are strong evidences of the classical band-like transport.
2. **Polaronic transport** (Holstein 1959[10] and Emin 1982[11]). In this regime, the charge carriers are self trapped in an initial site and transfer to another neutral site by tunneling, due to the lattice vibration. In the single-crystal rubrene OFETs, the application of high pressure tunes the intermolecular distance and leads to a linear increase of the carrier mobility with increasing the pressure.[12] This is in agreement with the Holstein-type small polaron model, which predicts that the mobility should be proportional to the square of the transfer integral and thus linearly increases with pressure for small variation in the intermolecular distance. The resulting mobility by this transport model is small, comparable to that by phonons assisted hopping, as discussed below.
3. **Hopping (variable range/energy hopping, nearest neighbor hopping)** (Mott 1979 [13]). In very disordered system, a large number of localized states distribute in the band tails where the charge carriers cannot move freely and only transfer by hopping, either in nearest neighboring localized states(nearest neighbor hopping) or to the smallest barrier sites(variable range/energy hopping). Hence the manifesting mobility is very small, often less than 1 cm^2/Vs. As the hopping rate can be enhanced by phonon vibrations, sometimes it is called phonon-assisted hopping, and the observed mobility shows a thermal activation behavior, i.e., $d\mu/dT>0$ or $\mu\sim\exp(-E_a/kT)$, where E_a is the average activation energy(usually in the range of dozens to hundreds of meV),[14] kT is the thermal energy. At ultra low temperatures, thermal activation is negligible and the carrier mobility will fall down to zero. The two features are usually used to identify the hopping transport. Furthermore, owing to the existence of hopping barrier, the relevant carrier mobility is strongly dependent on the position of Fermi level in the band. As the Fermi level moves over the energy level of localized states, the hopping barrier decreases because of deep traps filling and finally, the mobility increases while the

Fermi level is rising. This feature is the reason for the gate-voltage or carrier-density dependent mobility in amorphous and polycrystalline organic transistors.[7]

4. **Multiple trapping and release** (MTR, Vissenberg 1998[15]). In the work of Horowitz,[16] he mentioned that MTR had been used to account for the gate-voltage dependent mobility in hydrogenated amorphous silicon proposed by Shur,[17] and afterwards was applied to explain the temperature dependent mobility in sexithiophene (6T).[18] At the beginning of the study of organic transistors, the organic semiconductors are mostly amorphous or polycrystalline, and a large quantity of traps lies in the band edges, or in the band-gap. The carriers move in the delocalized states band as band-like transport but degraded by the populated traps at the band edges, hence the carriers are dynamically trapped into and released from the trap sites (shallow traps), reducing the apparent or average carrier mobility.[7] An important feature of MTR is that it could be used to determinate the density of states (DOS), and there have been a number of reports, e.g. for a-Si and 6T.[18] This kind of carrier transport is very similar to the thermally activated hopping and the carrier mobility also exhibits a thermal activation behavior. By MTR transport, the mobility in organic transistor often shows a power law dependence on the gate voltage.

Generally, the organic semiconductors are intrinsic, which means that both electrons and holes can contribute to the conduction but their mobility are quite different. Alike the classical semiconductors, the organic semiconductors can be classified as p-type and n-type, depending on which kind of charge carriers mainly contributes to conduction. However, this classification is not determined by doping but rather relevant to the charge injection. Owing to the majority of metal which could be used as the contacting electrode often possesses high work functions, thus the holes are easier to be injected from the contacts into the organic film, whereas the electrons have to overcome a large barrier to reach the LUMO due to the wide band-gap of OSC, typically at the level of 2-3eV. The efficiency of electron injection is thus very low compared to that of holes and the carrier transport is dominated by holes. Therefore, most of OSCs and most of organic transistors are p-type.

An example is shown in Fig. 1.3, for a transistor using pentacene and gold as the active semiconductor and the contact material, respectively. It is clear that the Fermi level of the gold contact is very close to the HOMO of pentacene, the barrier for the hole injection is much less than that for the electrons. Thereby, the pentacene and the pentacene-based OFETs with gold contacts are generally p-type. More examples with various organic semiconductors and different contact materials can be found in Ref.[19] In fact, the injection barrier is affected by many factors, such as the metal-OSC dipolar interface which will be discussed in the next chapter. Another interesting topic on decreasing the electron injection is by introducing traps in OSCs, which distribute at the OSC/contact interface and over large energy range, i.e. close to the LUMO. The electrons are not directly injected through a large barrier but rather accomplished by the traps transit.[20]

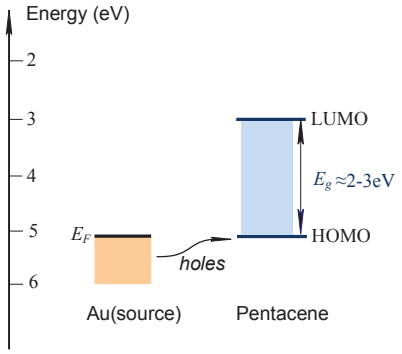

Figure 1.3 | Band diagram of a contact pentacene. Because the Fermi level of the contact of gold is closer to the HOMO of pentacene, the holes are easier to be injected into the HOMO of the pentacene film as compared to the electron injection.

If one applies a metal of small work function as the contacting material, e.g. Ca, the electrons can be also easily injected into the LUMO of OSCs, the OSCs and thus the accordingly based organic transistors will be n-type. Therefore, the classification of p/n type of OSCs is meaningless, and it relies more on the external or extrinsic conditions.[6] It has also been reported

that the electrons and the holes could be injected into OSCs simultaneously. This is the so-called ambipolar conducting feature and is useful for the electroluminescent devices, such as OLED, because the light-emitting efficiency depends on the recombination of n-type and p-type charge carriers. Unfortunately, the ambipolar conduction is still a severe challenge,[5] because the density of n- and p-type traps should be minimized simultaneously and the effective injection of both electrons and holes should be realized. In fact, the presence of traps that ***selectively*** capture either electrons or holes cannot be excluded, for instance in the time of flight(TOF) measurement on single-crystal penylene OFETs, the electrons and the holes exhibits comparable high mobility in the pristine condition, but in the air, those OFETs show a unique hole conduction. This might be due to the presence of oxygen in the crystal, which is known to act as a trap of electrons. The organic single-crystals with their intrinsically low density of traps (which are mostly distributed at the interface of OSC/dielectric), offer a unique opportunity to realize and to observe ambipolar operation with a relatively high mobility of both carrier types. From another point of view, to improve the two injections at the same time, the OSCs of smaller band gap (e.g. FePc, CuPc and rubrene) become important since it permits the electrons and the holes to be effectively injected from the source and drain electrodes, which could be a same metal. The mobility observed in the single-crystal of these materials was 0.3 cm^2/Vs and 0.03 cm^2/Vs in FePc, for holes and electrons, respectively.[21] The mobility in single-crystal rubrene could attain 1.8 cm^2/Vs and 0.01 cm^2/Vs for holes and electrons, respectively.[22] However, the CuPc based single-crystal OFETs show only p-type conduction, this might be because the high density of n-type traps limit the electron transport.[23] Meanwhile, we notice that the widely used complementary MOS (CMOS) structure needs p-type and n-type transistors simultaneously, but the different type of transistors should be separate, i.e., the ambipolar transport in one transistor cannot be applied for the CMOS circuit.[24]

Doping is also feasible for organic semiconductors, but it is only to improve the bulk conductivity and the mobility. After several tries, this method is no longer used now. This is because the organic transistors are generally thin-film transistors (TFTs), in which the intrinsic semiconductor thin film having very low natural conductivity is necessarily required to switch off the channel at small gate bias, in contrast to the classical silicon MOSFETs in which the reversely polarized p-n junction between the contacts and the channel leads to very slight leakage current at the "off" state. Therefore, even though the doping increases the mobility it will significantly increase the "off" current and thus diminish the ratio I_{on}/I_{off}. The typical dopants for OSCs are polyaniline (PANI) and poly (3-4-ethylenedioxythiophene) PEDOT/PSS.

Inorganic semiconductors have high carrier mobility, but the based devices necessitate high processing temperature and complicated, expensive equipments. In organic semiconductors the carrier mobility is several orders of magnitude lower, but the drawbacks of inorganic devices could be overcome by using organic semiconductors because of their possibility of low processing temperature and low cost. So, is it possible to benefit the advantages of the two different materials in a material? The answer is the so-called organic-inorganic hybrid material, which combine the useful properties of both organic and inorganic materials within a single molecule-scale composite. Organic-inorganic hybrid materials show very interesting magnetic, optical, structural and electrical properties.[25] A good example of optical material is made by successive vacuum deposition of amorphous copper phthalocyanine and titanium oxide layers, obtaining a photoconductive composite with a response much higher than that observed in single layers of copper phthalocyanine, probably due to the higher probability of charge separation at the organic-inorganic interface.[26] Electrostatically layered hybrid multilayer structures consisting of alternative layers of positively charged (photonated) poly (allylamine) or PPV and negatively charged CdSe nanocrystals have achieved a broad electroluminescence (EL) spectrum,[27] which can be further refined and tailored by selecting nanocrystals of different size.[28] A rectifying device (e.g. Zener diode) was similarly prepared with using a two-layer configuration comprising a p^+-doped semiconducting polymer [polypyrrole or poly(3-methylthiophene)] layer and a n-type

multilayer structure of CdSe (capped with trioctylphosphine oxide) and 1,6-hexanedithiol. By appropriately controlling the doping level in the p-doped polymer, an asymmetrically doped junction can be obtained, exhibiting rectifying behaviors under forward bias and Zener breakdown at reverse bias.[29] More details could be found in the book "*Thin Film Transistors*", chapter 10.[30]

1.2 PRINCIPAL PARAMETERS

Carrier mobility and conductivity are two principal parameters for organic semiconductors.

■ Mobility

Mobility characterizes the carrier speed in a solid under an electrical field. Microscopically, the charge carriers are accelerated by the force induced by the applied electrical field, at the same time they are periodically scattered by the scattering centers, e.g. phonons. This process occurs rapidly and across a large number of carriers which averages the observed effect, all the carriers exhibit a mean free path and mean velocity, the latter is described by mobility, μ (cm^2/Vs), as stated above. There are numerous methods to probe the carrier mobility in organic semiconductors, such as conductivity or resistivity, Hall Effect and time of flight (TOF), each method has a different physical meaning. These obtained carrier mobilities are microscopic and describe the intrinsic carrier mobility in their respective band, hence different from those in organic transistors. For instance in the next chapter, we will discuss the low-field mobility, the effective mobility and the field-effect mobility. Note that, the mobility obtained by TOF might be substantially different from that found in a real transistor because the carrier density in TOF measurement is very low, contrasting to the high density in transistor, particularly at high gate biases. It should also be mentioned that TOF is not sensitive to the contact effects in OFETs because the charge carriers are photon generated, not injected from a metal electrode.

Of course, mobility is the most important parameter to evaluate the OSCs' and thus OFETs' performance. A higher mobility will provide stronger current at a fixed bias, the shorter switching cycle and the higher ratio of I_{on}/I_{off} of transistors. Unfortunately, the mobility in organic semiconductors still remains at a very low level as compared to their inorganic counterparts, in which the mobility can reach to 10^4 cm^2/Vs in the direct band-gap semiconductors, e.g. single-crystal GaAs. This is due to the OSCs' intrinsic characteristics (e.g. narrow band width), impurities and the structural defects during the fabrication and etc. In a transistor, the influences on mobility become more complex, e.g. the quality of interfaces, in particular the OSC/dielectric interface. This kind of complexity arising from extrinsic influences makes the carrier transport mechanism is quite complicated there. In an ideal case, the carrier mobility of each type of transport corresponds to its own feature, e.g., the negative temperature dependence of mobility corresponds to the band-like transport in delocalized states whereas the positive one corresponds to the hopping transport in localized states, similarly for the gate-voltage dependences (will be discussed later). The com-

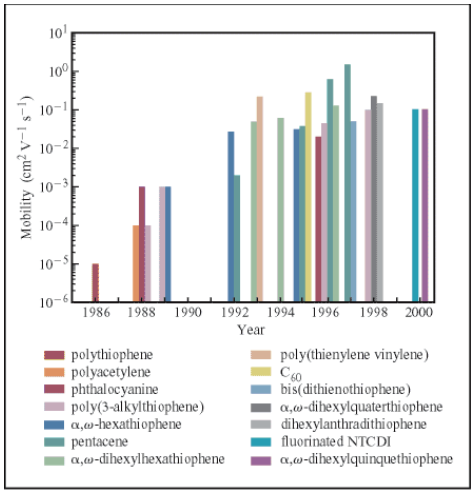

Figure 1.4 | Semi-logarithmic plot of the highest field-effect mobility reported in the organic transistors fabricated from the most promising materials versus year from 1986 to 2000.(after Dimitrakopoulos 2001 [3]).

bination of the two kinds of transport could explain the observed temperature independent mobility in high quality pentacene OFETs.[31]

Examining the evolution of mobility in the past two decades, one can find that the improvement of mobility was made by either the syntheses of new materials or the progress of the fabrication technologies. Fig. 1.4 shows such a process. With the appearance of various new materials, the mobility in pentacene was increased several times, which was achieved by the new technologies. Therefore, one can still expect further improvement of mobility towards its intrinsic value in this typical material.

Interestingly, there are some works reporting that the intra-molecule[3] or intra-grain[32, 33] mobility is much higher than those obtained in the bulk of OSCs. This is because a bulk of OSC in an OFET of micro-size channel length generally contains a large number of molecules and grains, where the carrier transport is taken place through several macromolecules and individual grains, thus the overall carrier mobility is limited by the lowest one resulted from the hopping transport inter molecules and inter grains. However the carrier transport within a single molecule or a single grain is much more efficient, for example, it is known that the mobility along the long axis of conjugated conducting and semi-conducting polymers (e.g. polyacetylene) can reach up to 1000 cm^2/Vs and even more.[3] Such a high mobility is clearly much desired for high performance OFETs, and it could be achieved by bridging the gap between source and drain electrodes with a single macromolecule or a single grain, corresponding to intramolecular and intra-grain transport. Note that the origins of low mobility in the two cases are different. For the inter-grains case, the large quantity of deep traps at grain boundaries are responsible for low hopping rate and thus low mobility. For the inter-molecules case, the low mobility is due to the weak van der Waals force interacting among nearest-neighbor (nn) molecules, the relatively strong lattice vibration significantly affects the inter-molecular transport. So one can improve mobility by strengthening intermolecular interaction (e.g., creating a stronger bond between nn molecules without breaking the molecular conjugation), leading to stiffer crystalline structures and thus less impact on the intrinsic carrier transport (e.g., band-like transport in delocalized states within a single macromolecule). Thus, one can obtain a high mobility at room temperature as that can be only observed at low temperatures, where the band-like transport mainly contributes to the overall conduction. Therefore, the structural organization of molecules plays an important role in the overall transport process. To attain a mobility as high as possible, the molecules should remain fully planar and parallel to each other, be in the closest possible packing and with the longest possible range order in order to prevent the formation of grain boundaries. The amelioration ways could be 1) the variation of experimental conditions used for film deposition, e.g. well control the substrate temperature and deposition rate; 2) tailoring the molecules in order to induce self-assembly properties; 3) growth of single-crystal OSC, in which the encouragingly high mobility with significantly reducing the structural defects has been observed.[5] All of these results imply that the study of mobility and thus the carrier transport should distinguish all the external influences first, such as traps. A detailed investigation of mobility in OSC and OFETs will be done in the forth chapter.

■ Conductivity

Brown *et al.* found that there exists a relationship between mobility and conductivity: $\mu \sim \sigma^{\delta}$ (δ=0.7~0.8),[34] for the OFETs with amorphous organic semiconductors, e.g. tetracyanoquinodimethane(TCNQ) doped with tetrathiofulvalene (TTF), poly (β'-dodecyloxy(-α,α'-α',α''-)terthienyl) (polyDOT$_3$) doped with 2,3-dichloro-5,6-dicyano-1,4-benzoquinone (DDQ) in this work and other data in the literature. It was found that the conductivity in the range of 10^{-7}-10^{1} S/cm follows a simple power relationship with the dopant concentration (N_D) as: $\sigma \sim N_D^{\gamma}$ ($\gamma \approx 4.5$). In amorphous OSCs, the carrier transport is by hopping (variable range hopping there) and thus one obtains: $\sigma = 2q^2R^2\nu_{ph}N(E_F)\exp[-2\alpha R(-E_a/kT)]$, where q is the electron charge, R is the hop

length, v_{ph} is a factor depending on the phonon spectrum, $N(E_F)$ is the density of electronic states at the Fermi level, E_a is the energy difference between the initial and final states and α is an electronic wave function overlap parameter. Doping increases the $N(E_F)$, and thus improving the hopping rate. At the same time, the hop length R decreases with doping, leading to also higher hopping rate and improving the mobility. Recall the relation: $\sigma=nq\mu$, where n is the mobile carrier concentration. If there exists a simple relationship between the mobile carrier concentration and dopant concentration as $n=\lambda N_D$, we will have $\mu\sim\sigma^{[(\gamma-1)/\gamma]}$. Associating all relations one can find that, $\delta=0.76$ will give $\gamma=4.2$, which is close to the value $\gamma=4.5$ stated above. It implies that in amorphous OSCs both conductivity and mobility are dependent on the dopant concentration. Meanwhile, the factor was found $\lambda=0.01$, which means that only a very small fraction of the introduced dopant contribute to conduction, most of them might be "self-trapped" or "pinned" to their dopant counter-ion. Furthermore, Brown *et al.* analyzed the impact on the ratio of I_{on}/I_{off} in OFETs and found $I_{on}/I_{off}\sim1+C_iV_D(\mu/2\sigma t_{SC})$, where C_i is the unit area capacitance of gate dielectric, V_D is the drain voltage and t_{SC} is the OSC film thickness. We notice that the doping increases mobility and conductivity simultaneously, however conductivity increases faster than mobility due to $\delta=0.7\sim0.8$ and actually, the ratio of I_{on}/I_{off} decreases with doping. This inference is important to explain the unfeasibility of improvement of OFETs' mobility by doping since it significantly degrades I_{on}/I_{off}, a critical parameter characterizing the OFETs' current modulation capacity.

Next, this relation between conductivity and mobility in amorphous OSCs was developed by Passch *et al.*,[35] with using Mott's variable range hopping in one-, two- and three-dimensional system. Their results well explain the conductivity dependences on temperature and on doping concentration, in particular on the mobility.

Garnier *et al.* found that in the oligomers of thiophene,[36-38] mobility and conductivity increase with the length of molecule chains (mobility increases more rapidly). Furthermore, the anisotropy of conductivity along different direction, i.e., $\sigma_{\text{parallel}}/\sigma_{\text{perpendicular}}$ with σ_{parallel} being the film conductivity parallel to the substrate, exhibits different property, implying the anisotropy of carrier transport in the OSC film. For instance, the transport parallel to the substrate plane (i.e., along the stacking axis of the oligomers), is enhanced with increasing the substrate temperature. This anisotropy is even more pronounced in the dihexylsexithiophene (DH6T), where the alkyl chains forming insulating layers strongly affect the perpendicular conductivity. It was also found that the absolute value of conductivity decreases as the substrate temperature is increased, and this decrease is drastic when the OSC materials form single-crystal structure. This means that the absolute value of conductivity is mainly determined by the material purity. So, by using very high purity OSC materials, one can realize very high dynamic ratio, i.e. large I_{on}/I_{off} values. For instance, the I_{on}/I_{off} as high as 10^7 was obtained in highly pure 6T film with sweeping the gate voltage from +10V to −40V.[39] In the end, one can find that the OSC conductivity is closely linked to the mobility, however sometimes they are a pair of contradictions, because the desired higher mobility will lead to higher conductivity but higher ratio of I_{on}/I_{off} in organic transistors necessitates the lower bulk conductivity. That's also why in the literature the mobility is often reported with the concurrently measured I_{on}/I_{off}.

1.3 MATERIALS OF ORGANIC SEMICONDCUTORS

The small molecular semiconductors and oligomer are constituted of finite number of monomers and on the contrary, the organic semiconductors of polymer contain numerous monomers.

■ Small molecular materials and oligomer OSCs

The typical small molecular OSCs are pentacene, rubrene and oligothiophene (abbreviation of nT, n represents the number of thiophene units). Others have the group of acene: such as tetracene (n=2, pentacene is also in this group with n=3), perylenediimides, TCNQ, fullerene(C_{60}) etc. The highest mobility is generally obtained in the OFETs with OSCs of small molecular materials.

This kind of materials is often deposited in vapor phase. The arrangement of molecule is very sensitive to the adjacent surface (e.g., the commonly used SiO_2), the interface quality is not good, exhibiting a disordered crystalline structure. Hence the transport at this interface will be trapping limited and the observed mobility is very small. Interestingly, as the temperature of deposition is increased[40] and/or the depositing rate[41] is decreased, such imperfect phenomena will be much improved. However a better way is to insert a self-assembled monolayer (SAM) between the OSC/dielectric, which not only improve the molecular organization close to the interface (facilitating the carrier transport) but also reducing the interface states, which might also play an important role in the overall carrier transport in organic transistors. Octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HDMS) over SiO_2 have shown very good results. For instance, a mobility as high as 6 cm^2/Vs was observed in the ultra-thin film of polystyrene (PS) by using such a strategy. However, Burgi *et al.* stated that HDMS improves the field-effect mobility at the interface of polymer/ SiO_2 but not the mobility in the bulk of the organic film.[42] At the same time, the polymer dielectric or SAM layers have been widely used to replace the conventional inorganic gate insulator, a higher mobility is obtained in the corresponding OFETs due to the better interface quality resulted from the similar characteristics between polymer OSCs and polymer dielectric.[43]

Another issue regarding the small molecular materials is the indissolubility but solubility is a very important feature to apply the low-cost solution-based technologies, e.g. roll-to-roll printing. There are some studies devoted to the application of precursors by grafting some solution groups, and then transform to the desired OSCs. More discussions will be done in the following text.

■■ Pentacene

At present, pentacene is the most popular material used as the active semiconductor in the current organic electronics. The unique features of this acene are the nature of its native solid-state order and its order in crystalline films (cf. Fig.1.5b), which is dominated by strong two-dimensional edge-to-face interactions, leading to a "herringbone" molecular organization. In evaporated films, pentacene is deposited with its long axis roughly perpendicular to the substrate, resulting in strong two-dimensional interactions parallel to the substrate (cf. Fig. 1.5c). Disadvantages of using pentacene in organic electronics are its insolubility as others small molecular OSCs, and the susceptibility to degradation by several pathways: including end peroxide formation and "butterfly" dimerization. The dominant edge-to-face arrangement of the pentacene molecules in the solid state may limit its electronic properties because the face-to-face interactions are predicted to induce stronger electronic coupling between molecules. With regard to the insolubility of pentacene, there are several methods to overcome this draw-

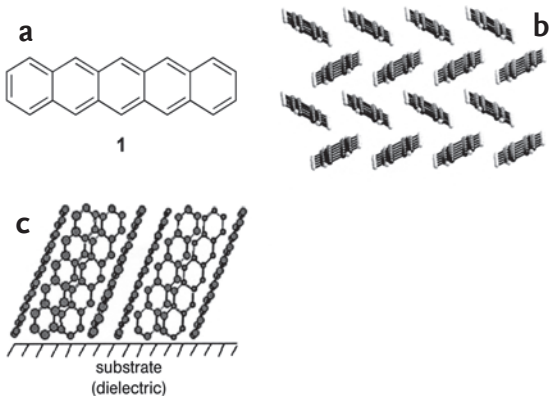

Figure 1.5 | (a) Molecular structure of pentacene, (b) crystalline order and (c) thin-film orientation of pentacene. (after Anthony 2006, in the book "*Organic Electronics*",[1], P59)

back. As discussed above, one method consists of the synthesis of a soluble precursor, which after film formation is converted into the active form upon heating.[44] An alternative is by substitution of the primary structure with solubilizing side groups.[45]

Pentacene OFETs showing holes conduction with a mobility over 1 cm^2/Vs had been reported in 1998 by Nelson *et al.*,[31] higher mobility of 3 cm^2/Vs was reported in the pentacene OFETs with polymer dielectric,[46] and a mobility as high as 60 cm^2/Vs was also found in the single-crystal pentacene OFETs.[47] At the same time, the functionalization of pentacene has also been applied to alter its solubility and improve the electronic performances, even effectively change its conduction type from p-type to n-type. This enables a new strategy to improve the performances of pentacene-based OFETs because the conventional methods to achieve those improvements are mostly by the optimization of the film deposition conditions, or by improving the film morphology and the OSC/dielectric interface quality as well as by repeatedly purifying the materials. All these methods are devoted to reduce the extrinsic influences but there will exist a limit of intrinsic performances of pentacene. Therefore, new materials design and synthesis are viable alternatives for pushing pentacene-based OFETs to a new performance level. The first use of functionalized pentacene OFETs was reported in 2003.[48] In that work, the molecular structure of pentacene (see Fig. 1.5a) is modified by introducing methyl groups in the 2,3 and 9,10 positions of hydrogen atoms terminal in the central ring, leading to tune the electronic properties of pentacene with the electron-donating ability and small size of methyl substituents. More details on the functionalization of pentacene can refer to ref.,[1] chapter 3: "Engineered pentacene".

Oligothiophene

After pentacene, the second most intensively studied class of oligomers for OFETs applications are oligothiophenes, basing on the thiophene ring, an electron rich heterocycle among which sexithiophene (6T) and hexyl-substituted thiophene oligomers (e.g. DH-6T and DH-4T) are the most investigated examples. In general, the unsubstituted oligothiophenes are poorly soluble and thus difficult to be purified and processed, however the alkyl-substituted oligothiophenes at the β core positions can be sufficiently dissolved in organic solvents, and thus facilitating the purification process. Alkyl-substituted oligothiophenes can be either end-group-functionalized (α-ω-functionalization) or side-group-functionalized (β-functionalization).[4]

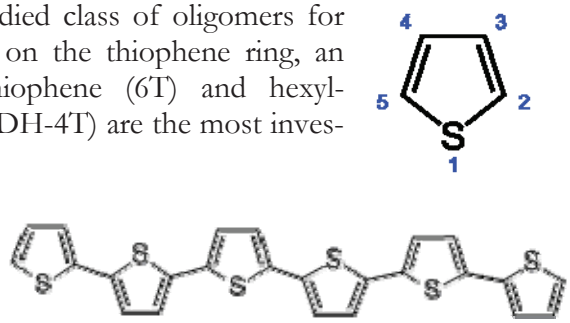

Figure 1.6 | Molecular structure of thiophene ring (upper), and sexithiophene (lower)

The OFETs based on 6T and DH-6T were first studied by Garnier *et al.*, the mobility was found to be around 0.002 cm^2/Vs[49] and 0.05 cm^2/Vs,[37] respectively, comparable to that observed in polycrystalline OFETs. They also proposed the strategies to improve the OFETs' performances: 1) employing rigid, rod-like molecules, such as thiophene oligomers with large π-conjugation lengths extending along the molecular axis; 2) close molecular packing of the molecules along at least one of the short molecular axes (π-stacking). The α-ω-substitution improves performances because it induces a higher degree of film organization. The β-functionalization has not been applied to a large degree because very small mobility was observed ($<10^{-7}$ cm^2/Vs) in the first β,β'-dihexylsexithiophene (β,β'-DH-6T) in comparison with DH-6T. This is due to the reduced tendency of the β,β'-substituted compounds to self-organize in the solid state. An issue associated with the use of electron-rich oligothiophenes is their ease of oxidation (doping) in air because of their high HOMO energies, which can be lowered by replacing some thiophene with phenyl rings.

TABLE 1.1 Summary of the OFETs' performance of some small molecular OSCs (p-type)

Semiconductor	Mobility (cm^2/Vs)	I_{on}/I_{off}	Notes	Refs.
Rubrene (air, PMMA)	1.5-20	NA	PDMS, SS=2nF.V/decade.cm^2,	[50]
Pentacene (SiO_2)	1.5	10^8	Photolithography, $V_T \approx 0$V, SS=1.6V/decade	[51]
Pentacene (PVP-CP)	2.9-3.0	10^5	Spin-coated PVP-CP, SS=1.2V/decade,	[46]
Pentacene (Al_2O_3)	0.06-0.1	10^6	Al_2O_3 prepared by Anodization	[52]
Pentacene (SiN_x)	0.2-0.55	10^8	Smooth PECVD,	[53]
Pentacene (Ta_2O_5)	0.45	75	Anodized and e-beam evaporated, SS=0,56/decade	[54]
Pentacene (Gd_2O_3)	0.1	10^3	Ion beam assisted deposited Gd_2O_3, ε=7.4	[55]
Pentacene (TiO_2+PαMS)	0.8	10^4	Anodized TiO_2, for one volt operating OFETs	[56]
Pentacene (BZT or BST)	0.32-0.6	10^5	Low operating voltage≈5V	[57]
Pentacene-precursor (SiO_2)	0.01-0.2	10^5	Spin coated pentacene from precursor solution	[44]
Pentacene-precursor (SiO_2)	0.89	10^7	By Diels-Alder reaction with N-sulfinylbutylcarbamate	[58, 59]
6T (SiO_2)	0.002		Combination of the substituted 6T	[37]
8T (SiO_2)	0.33 (T>120°C)		Grown at various substrate temperatures,	[60]
DH6T (SiO_2)	0.05	10^3		[37, 61]
DH4T (SiO_2)	0.06	10^6		[61]
Single-crystal silicon	500-1400			
Polycrystalline silicon	50-100			
Amorphous silicon	~1			

The materials in the brackets after semiconductors are the gate dielectric. (some data after Facchetti, 2007[62])

■ Polymer OSCs

The typical polymer OSCs are polythiophene, especially poly 3-hexylthiophene (P3HT), and polyfluorene, polydiacetylene, poly 2,5-thienylene vinylene, poly p-phenylene vinylene (PPV), polytriphenylamine (PTAA), copper phthalocyanine (CuPC) etc. They could be simply classified as conjugated polymer and regioregular polymer. The conjugated polymer was developed at the beginning of the study of organic semiconductors based on the existing techniques. Nearly all conjugated polymer are p-type semiconductors.

In general, the polymer based OFETs show lower performances than those of small molecular OSCs. With regard to polymer OFETs, regioregular polymers exhibit better performances than conjugated polymers. The work of Sirringhaus *et al.*[63] reveals that the low level of polymer OFETs' performances are due to two factors: 1) chemical impurities which lead to a large number of traps in the organic film; 2) structural disordering, which causes a lot of defects and limits the carrier transport. More details on the carrier transport in solution-processed polymers (and other OSCs) could be found in ref.[64]

Despite the relatively low performances, polymers are perfectly suitable for the solution-based process, targeting at the low-cost flexible organic electronics. This is due to the facts that the resulting polycrystalline films of small molecules are often susceptible to mechanical stress, even though they could also be deposited by solution-based techniques. However, polymers generally have very good solubility and processability, which are important features to form a good-quality film over large surface on a flexible substrate.

■■ Polythiophenes

Polythiophenes are the mostly investigated polymers for OFETs applications. This is because they combine both advantages of small molecules and polymers, e.g. very low "off" conductivity but with high field-induced carrier mobility in the "on" state, as well as good flexibility and low specific mass.

The unsubstituted polythiophenes are difficult to be dissolved in common organic solvents. The first demonstration of the unsubstituted polythiophenes based OFETs was reported in 1986

by Ando *et al.*[65] A saturation field-effect mobility was found around 10^{-5} cm^2/Vs with I_{on}/I_{off}=100-1000 in bottom-gate configured OFETs. To improve their insolubility, alkyl chains are introduced into the 3-position of the thiophene monomers, at the same time obtaining longer chains which form more uniform polythiophene layers. Soluble poly(alkylthiophene)s (P3ATs) were first reported in 1985.[66] Due to the non symmetric monomers in 3-alkylthiophenes, there are three possible coupling patterns of dimeric subunits in the polymer chain if the thiophene building blocks are connected solely in the 2- and 5- position, as shown in Fig. 1.7(upper). They are 2,5'-or head to tail (HT) coupling, 2,2'- or head-to-head(HH) coupling and 5-5' or tail-to-tail(TT) coupling. The coexistence of the three coupling in P3ATs causes the limitations on the intramolecular electronic conjugation in the chain and on the intermolecular interaction in the solid state and thereby, the regioregular P3ATs with continuous HT coupling are much desired. A mobility up to 0.1 cm^2/Vs was obtained in the OFETs with highly regioregular P3HT processed from chloroform.[23, 63] It is believed that the regioregular P3ATs are partially crystallize in laminar layer domains, in which the layers of "surface-to-surface" stacked polythiophene "main chains" are separated by layers of isolating alky side chains. As shown in the lower figure of Fig. 1.7, the highly regioregular P3ATs often form a laminated structure with a vertical arrangement of the thiophene molecular axis relative to the substrate, i.e., the π-π stacking alignment is parallel to the substrate.[63] A study comparing P3ATs with different alkyl side chains showed that the carrier mobility decreases with increasing length of the alkyl chain, and it is attributed to the isolating properties of the alkyl side chain.[3] Next the investigation of influences of P3HT molecular weight on the OFETs mobility was conducted, and it was found that the mobility dramatically increases with the P3HT molecular weight.[67, 68] The layers of low molecular weight P3HT show more crystalline at first since individual, extended crystallites are observed by AFM on the corresponding thin film and moreover, a very high order in the chains within these crystallites is confirmed by diffraction experiments. However, such good order and individual crystallites cannot be observed in the film of high molecular weight P3HT. The low mobility in small molecular weight fractions was attributed to the charge traps at the crystal boundaries of the crystallites. Furthermore, in the high molecular weight P3HT the ordered regions are connected actively and electronically along long polymer chains, whereas such connections are absent in the low molecular weight P3HT. Electronic isolation of the crystallites might be the reason for the significant drop of mobility in low molecular weight P3HT.

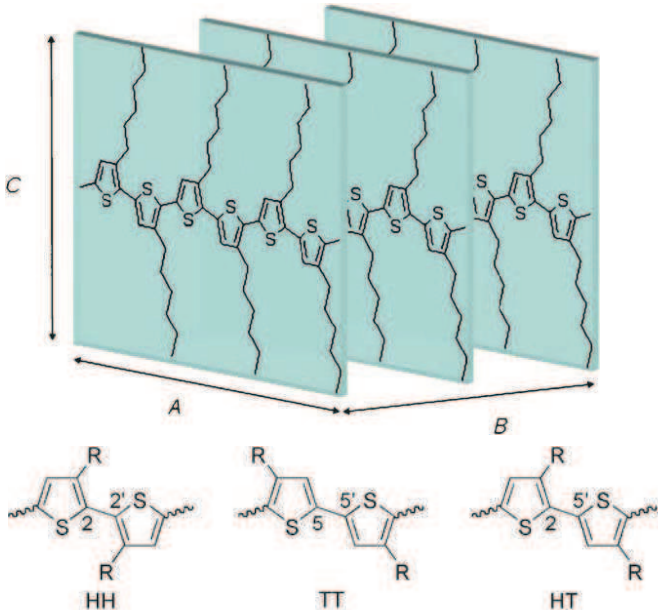

Figure 1.7 | Upper: Regioisomeric coupling patterns in poly(alkylthiophene)s. Lower: model for packing of P3HT in the solid state (A: orientation of the molecular axes; B: intermolecular stacking direction; C: orientation of the alky side groups). (after Allard 2007[4])

Alike thiophene, polythiophenes are also sensitive to oxidation due to the low ionization potential (typically less than 4.9-5.0 eV). This oxidation will cause a shift of the threshold voltage in the polythiophene based OFETs. This behavior is ascribed to the primary formation of loose, reversible "charge-transfer" complexes with oxygen (doping). In order to improve their stability, the ionization potential is increased by a distortion of the coplanar main-chain conformation (change in the substitution pattern of the side chain) or through the incorporation of non-conjugated comonomer building blocks into the main chains.[64] Till now, the above texts are

mostly devoted to the 3-position substituted polythiophenes, more details on the other types of polythiophene can be found in ref.[4]

Polytriphenylamines

In addition to sulfur-containing polythiophenes, nitrogen-containing aromatic polymers, polytriarylamines (PTAAs), have attracted interest for OFET applications in recent years. In fact, low molecular weight or oligomeric triarylamines are known as hole conducting materials for the active layers of photocopiers, OLEDs and organic solar cells. Apart from their advantages of high mobility and good stability towards air and humidity, PTAAs and the corresponding oligomers exhibit very good solubility in common organic solvents. With respect to P3HT, PTAAs based OFETs show lower mobility (10^{-3}-10^{-4} cm^2/Vs) but PTAAs are very promising candidates for solution-processable OFETs, reproducibly forming thin film of completely amorphous solid-state microstructure. In 2002, the PTAA was first used as active materials in OFETs.

Next, the poly(triphenylamine)s (PTPAs) were prepared by a metal-catalyzed aryl-aryl homocoupling of the dichloro monomers in the presence of nickel chloride/zinc. The mobility obtained by time-of-flight(TOF) is around 10^{-2} cm^2/Vs, but that obtained in the corresponding OFETs by I-V characterization in saturation regime is around 2×10^{-3} cm^2/Vs with I_{on}/I_{off}=2.3×10^5. In 2005, Hubler *et al.* reported the first printed OFETs based on PTPAs with significantly improved solubility and higher molecular weight, the saturation field-effect mobility was found at 3×10^{-3} cm^2/Vs with I_{on}/I_{off}=2×10^5.[69] Afterwards, an investigation of the stability towards oxidation of PTPA-based OFETs showed a significantly increased storage and air stability relative to fluorine/bithiophene copolymer(F8T2)-based OFETs. The PTPA-based OFETs could be stored in air for a year without change in OFETs properties, the mobility only decreases from 3×10^{-3} cm^2/Vs to 1.3×10^{-3} cm^2/Vs. However, the F8T2-based OFETs (initial mobility of 2×10^{-3} cm^2/Vs) lost OFETs behaviors after 2000 hours storage.

TABLE 1.2 Summary of the OFETs' performance of polymeric OSCs(p-type)

Semiconductor	Mobility (cm^2/Vs)	I_{on}/I_{off}	Notes	Refs.
P3HT	10^{-5}-0.1	10^2-10^6	High μ in BG OFETs[70]	[70-72]
PTAA	10^{-5}-0.01	10^3-10^5	Ultra thin TiO_2, for low operating voltage<1V, SS=0.2V/decade[72, 73]	[72, 73]
F8T2	10^{-5}->0.02	10^2-10^6	Highest mobility observed in BG OFETs with Si_3N_4 dielectric	[72]
PTPA on CYTOP	~10^{-3}		In TG OFETs	[4]
PTPA on PVP	~10^{-4}		In TG OFETs	[4]
PTPA on PMMA	~10^{-4}		In TG OFETs	[4]

Single-crystal OSCs

Actually, single-crystal (SC) organic semiconductors are not a new category of organic material and they are, in principle, comprised by the small molecular OSCs, such as pentacene and rubrene. Moreover, SC OSCs are not only limited into p-type semiconductors, the n-type SC OSCs are also available, e.g. single-crystal TCNQ. In the bulk of single-crystal OSCs, the arrangement of molecules is almost the same and moreover, there is not grain boundary and thus the defect density is very low compared to that in polycrystalline and polymer OSCs. As a result, the carrier transport is not limited by the extrinsic influences, such as the charge traps at grain boundaries in polycrystalline OSCs; a nearly intrinsic carrier transport is attainable in this type of OSCs. If they are applied as active layers in OFETs, the resulting transistors generally exhibit very high reproducibility because of the very low defect density. By applying diverse structure configurations and diverse dielectric materials, one can address the impacts from the choice of device structure and dielectric on the overall carrier transport. In consequence, the single-crystal and the correspondingly based OFETs are often used as an important tool for transport study. More details on the relevant issues can refer to refs.[5, 74, 75]

■ N-type OSCs

As comparing to p-type OSCs, n-type OSCs are rarely reported in the literature. There are so many reasons for such a result. The most accepted explanation is the large Schottky barrier for electron injection from most large-work-function metal contacts into OSCs. Apart from applying a low-work-function metals (e.g. Ca and Al), this problem can be improved by substitution of strong electron-withdrawing substituents in order to reduce molecule/polymer frontier molecular orbital energies so that electron injection/transport prevails. The second reason would be the relatively low carrier mobility with respect to p-type OSCs. This might be due to the higher density of electron traps in comparison with that of holes which selectively limits the effective mobility of electrons. This issue can be ameliorated by modifying the surface properties of the gate dielectric to eliminate electron trapping sites. By this way, electron transport is largely reported in many polymer OSCs which are previously thought to be exclusively p-type OSCs. This inference is further proved by a high mobility of 1.6 cm^2/Vs observed in the air-gap single-crystal OFETs of TCNQ processed by flexible elastomeric polydimethylsiloxane (PDMS) stamps.[76] Another issue concerning the application of n-type OSCs is the high sensitivity to air and humidity. This is due to the fact that the radical anions are chemically much less stable than radical cations. The first examples of n-type materials, e.g., TCNQ, C_{60}, C_{70}, have confirmed their high reactivity toward oxygen, which impede their application in devices operating under air. Thus a number of n-type OSCs having high electron affinity have been proposed, such as naphthalene tetracarboxylic dianhydride (NTCDA), and perylene tetracarboxylic dianhyride (PTCDA). A highly stable n-type semiconductor was developed in Lucent Bell Labs groups, by the full substitution of a phthalocyanine with fluorine substituents.[77, 78] The electron mobility in these n-type conducting materials was found to be highly dependent on the structural organization of the organic film, and the mobility values at the level of 10^{-2} cm^2/Vs were obtained in perfluorinated phthalocyanines and C_{60} in high vacuum. Up to now, stable n-type OSCs with high carrier mobility are still a severe challenge in the organic electronics community.

Many n-type OSCs are based on oligothiophenes in which the molecular energy levels have been tuned by substitution with cyano, perfluoroalkyl/aryl, and alkyl/arylcarbonyl. For example, Pappenfus *et al.* have reported that quinoimethane terthiophene (QM3T) shows n-type conduction with mobility 0.002-0.5 cm^2/Vs.[79] Facchetti *et al.* reported a high mobility up to 0.24 cm^2/Vs in perfluorohexylsubstituted thiophene oligomers.[80] More recently, oligothiophenes containing or substituted with carbonyl groups have been synthesized. One compound of this family is an air-stable n-type oligothiophene (DFHCO-4TCO) with electron mobility of 0.01 cm^2/Vs, however other systems exhibit very high electron mobility in vacuum both as vapor-deposited (DFHCO-4T, μ~0.6 cm^2/Vs) and as solution-case (DFPCO-4T, μ~0.24 cm^2/Vs) films.[81, 82] Another group of electron conductors is based on fused acenes such as naphthalene and perylene. Naphthalene carbodiimide (NTCDI) derivatives, which are synthesized from NTCDA and amines, were first studied by Katz *et al.*[83] The unsubstituted systems show relatively low mobility, while the incorporation of fluoroalkyl groups stabilizes NTCDI electron transport in air.[78] More recently, N,N'-dialky substituted perylenetetracaboxydiimide derivatives (PDIs) have been intensively studied. A record electron mobility of 2.1 cm^2/Vs was reported for PDI13 after annealing at 140°C.[84] Fullerenes (C_{60}-C_{70} 9:1 mixture) are also an important type of n-type OSCs. The corresponding OFETs were first studied by Kasner *et al.*, the electron mobility was found around 10^{-4} cm^2/Vs. C_{60} has an isotropic molecular structure and thus forms isotropic solids, resulting in a good quality film without needs to control molecular orientation as in other OSCs. Haddon *et al.* have reported excellent device characteristics for C_{60} films deposited in ultrahigh vacuum with mobility up to 0.08 cm^2/Vs and I_{on}/I_{off}~10^6.[85]

TABLE 1.3 Summary of the OFETs' performance of n-type OSCs (some data after Facchetti, 2007[62])

Semiconductor	Mobility (cm^2/Vs)	I_{on}/I_{off}	Notes	Refs.

QM3T	0.002~0.005	~10^5	Solution/vapor deposited, on SiO_2 with Ag contacts(TC, BG)	[79]
DFH-4T	0.24	10^8		[61]
DFHCO-4TCO	0.01	10^6	Vapor deposited on HMDS treated SiO_2 with Au contacts(TC, BG)	[81]
DFHCO-4T	0.6-2	~10^3	Same as above	[81]
NTCDI (8-18)	0.005-0.16	10^3-10^6	Spin-coated on SiO_2 with Au contacts	[83]
PDI8	0.6	>10^5	Vacuum evaporation with Au contacts, BC and BG	[86]
PDI13	2.1	~10^5	Thermal evaporated on SiO_2 with Au contacts, TC and BG	[84]
C_{60}	10^{-4}-0.08	10^2-10^4	Thermal evaporated on Al_2O_3 with Al(G) and Mg(S/D) contacts	[87]
C_{60} (on pentacene)	2.0-4.9	~10^3	Same as above	[87]
TCNQ (air-gap)	1.6	NA	Single-Crystal, PDMS,	[76]

1.4 OTHER MATERIALS FOR ORGANIC ELECTRONICS

It is necessary to briefly introduce some important materials used in organic electronics because the fully organic transistors necessitate the dielectrics, electrodes, interconnections, substrate and even passivation layer also in organic material, but they are usually inorganic materials in the conventional devices. These new materials enable the low-cost, low temperature processed, flexible, transparent and little environmental pollution organic electronic products.

■ Organic dielectrics

The gate insulator is a key element in organic transistors because at high gate biases very high density of charge carriers are confined in a narrow channel close to the interface of OSC/dielectric, and thus the gate dielectric may play an important role in the overall carrier transport.[88, 89] This thin film of insulator should have high dielectric constant (in order to have higher capacitance and thus reduce the operating voltage) and very low density of mobile or localized charges (in order to improve the uniformity of threshold voltage). In addition, the gate dielectric sometimes determines the molecular growth and the molecular orientation during the deposition of the organic film, both for small molecular semiconductors and for pre-oriented, highly ordered semiconducting polymers. At the beginning of OFETs study, most of the used dielectrics are SiO_2 or other inorganic oxides (e.g. Al_2O_3, TiO_2, Ta_2O_5) but it is not compatible with the unique features of organic electronics, such as low-temperature process, flexible, transparent and moreover, it is difficult to make individual gate electrode with those oxides and thus difficult to make organic circuits. It should be noted that the inorganic dioxides of high dielectric constant are of interest implemented for the application of low power consumption or low voltage operation, however most of high-ε materials suffer from expensive deposition methods (sputtering) and poor film quality (requiring relatively thick films to reduce gate leakage). Furthermore, the mobility dependences on the gate dielectric constant seem contradictory. For example, in amorphous or polycrystalline OFETs the carrier transport is mostly by hopping, the effective mobility of overall charge carriers is strongly dependent of the carrier density. Higher-κ dielectric will give higher carrier density at same biases, thus improving the mobility. However, the mobility in single-crystal OFETs is found to be significantly reduced by using the higher-κ gate dielectrics, an empirical relationship between mobility and permittivity $\mu \approx 1/\varepsilon$ was proposed.[90] This might be due to the reason that dipole field present at the surface of high-κ insulators may enhance the formation of local states that in turn induce carrier localization and reduce charge-carrier mobility. Hence, benefits have resulted from use of low-κ organic dielectrics, more and more organic dielectrics are presently introduced to the OFETs fabrication and they

exhibit also good electrical characteristics, good mechanical and chemical properties as well as good processability.

TABLE 1.4 Summary of the gate dielectric materials used for OFETs application

Material	Preparation method	Dielectric constant	Notes	Refs.
SiO_2	Thermally grown	3.9	Deposition temperature >600°C	[46, 51, 91]
SiO_2	Ion beam sputtered	3.9	Deposition temperature ~80°C	[92, 93]
Al_2O_3	Sputtered	~5.1		
Al_2O_3	Anodized	~4.2	At room temperature	[52]
TiO_2	Anodized	21	At room temperature	[56]
SiN_x	CVD	6-7	Deposition temperature 250-350°C	[94]
BZT	rf sputtered	17.3	At room temperature	[57]
BST	rf sputtered	16	At room temperature	[57]
Ta_2O_5	Anodized/e-beam evaporated	29	Deposition temperature ~300°C	[54]
CYEP		18.5		
PVP	Ink-jet printed	4.5	TG, rubbed polyamide substrate	[95]
PVA		7.8-10		
PI	Printed		C_i=20nF/cm^2, P3HT	[96]
PMMA		3.5	TG	[97]
CYTOP		2.1	TG	[97]
Polypropylene		2.1	TG PTAA OFETs	[72]
Polyisobutylene		2.2	TG PTAA OFETs	[72]
CYMM		18	TG PTAA OFETs	[72]

For more data can refer to refs.[72, 80]

Polymers are of course the first potential materials for gate dielectric because of their native insulator properties. The solution-processable polymer gate dielectrics, the most promising dielectric materials, can be deposited by spin-coating, spray-coating or printing, from a polymer solution (polymer dissolved in a suitable solvent). Subsequently, by drying the film to evaporate the solvent or by an additional heating or irradiation step, the final film of polymer dielectric is formed. Typical examples of these polymers are polyimide (PI), polyvinylphenol (PVP), photoresists, poly (methyl methacrylate) (PMMA), poly (vinyl alcohol) (PVA), and the class of spin-on glasses (silsesquioxanes).

Contrasting to the "top-down" method of deposition of polymer solution, another "bottom-up" approach for polymer dielectric film forming is the "growth" of polymers from monomers directly on the gate electrode surface. A typical example is poly-***para***-xylylene (Parylene), in which the pyrolysis of a ***para***-xylylene dimmer generates radicals that polymerize on a substrate held at room temperature forming an insulating film. At present, parylene coatings are widely used in the packing applications, the equipment for its deposition is inexpensive and easy to build. This material with the dielectric constant ε=2.65 forms transparent pinhole-free conformal coating with excellent mechanical and dielectric properties, the breakdown electric field could be as high as ~10MV/cm for a thickness of 0.1μm. The important advantages of using parylene as the gate dielectrics are that: 1) it can be deposited while the crystal remain at room temperature, 2) being chemically inert, it does not react with other organic materials; and 3) the parylene/OSC interface has low density of surface states; 4) it has the comparable thermal expansion/contraction with most of organic materials due to its carbon-based polymer property, thus the resulting interface with OSCs is not sensitive to the stress-induced carrier trapping which is often encountered in the single-crystal OFETs with the gate insulator of inorganic oxides. (for more details on parylene can refer to ref.,[98] P411-P412)

One of the most critical problems in using OFETs is the high operating voltage because of the poor capacitive coupling through a thick gate dielectric (e.g. >100nm) to minimize the gate leakage. Self-assembled monolayer (SAM) is a promising approach to solve this problem. The thickness of SAM could be as thin as one molecular monolayer (around the length of a molecular) and moreover, the SAMs can withstand very high electric field up to 16MV/cm by using proper molecular design and deposition process, this electric field intensity is comparable to or better than those of thermally grown silicon dioxide dielectric of similar thickness.[99] Vuillaume *et al.* have reported SAMs with a solution-grafted monolayer from vinylterminated monolayer.[100, 101] The Infineon group has grafted modified alkoxysilane molecules directly on a briefly activated surface to obtain a high quality SAM without chemical conversion.[99] With both methods, functional OFETs with operating voltage as low as 2V could be reached.

The above discussed gate dielectric is using a single layer of one material, however multi-layer or multi-component systems could also be introduced to improve OFETs performances and to tune the electrical characteristics. The best-known example of a multi-layer dielectric system is octadecyltrichlorosilane (OTS) on silicon oxide. After treating the silicon oxide with C_{18} alkane, which forms a covalently bonded monolayer on the oxide surface with a silane anchor group, improved OFETs performances (mobility, threshold voltage, subthreshold slope and I_{on}/I_{off} ratio) and homogeneous distribution of OFETs properties on a substrate were obtained, for pentacene OFETs with respect to the ones on an untreated surface.[51] Kobayashi *et al.* even used this approach to successfully tune the threshold voltage over a wide range from positive to negative, by changing the nature of SAMs at the interface of OSC/dielectric.[102] Another well-known example is that the mobility in pentacene OFETs is increased by a factor of three as compared to the OFETs without treatment, by deposing a few nanometers thick of apolar polymers (e.g. PAMS-poly (α-methylstyrene)) on oxide surface.[56] Note that this improvement of mobility by treatment of the gate dielectric with organic materials (SAMs or polymers) is not due to the increase of grain size and thus the decrease of grain boundary, which is valid for oligothiophene [103] but is not applicable for pentacene.[53, 104]

In addition to the combination of inorganic dielectric with organic monolayers or polymers, the inorganic-inorganic and organic-organic multi-layers have also been investigated for a complex gate dielectric composite. An example of an organic double-layer dielectric system is the combination of a SAM layer with a polymer dielectric film (PVP), but with architecture opposite to that typically fabricated in SiO_2/OTS where the SAM covers the bulk dielectric. Integrated circuits (ICs) based on pentacene OFETs containing a double layer 2.5nm thick (18-phenoxyoctadecyl) trichlorosilane (PhO-OTS) followed by a 13nm thick film of cross-linked PVP can operate with supply voltage from 3 to 20V without electrical shorts, which could protect an OFET from surge currents, without losing the functionality at low voltage.

Most polymers have low dielectric constant (e.g. 2.5-4), depending on their molecular structure. To increase the capacitive coupling, addition of high-ε components to the polymer matrix is suitable with maintaining the layer-by-layer deposition discussed above. One example is the dispersion of high-ε nanoparticle (TiO_2) in a traditional polymer dielectric PVP, reported by Chen *et al.*[105] By adjusting the concentration of TiO_2 particles in the blend, the dielectric constant increases from 3.5 (in unmodified polymer) to 5.4 for the nanocomposite dielectric containing 7% nanoparticles, increasing the drain current of the pentacene OFETs. More details on gate dielectrics can refer to ref.,[1] chapter 6; as well as refs.[72, 80]

■ Organic electrodes or interconnections

Until now, the organic transistors are generally made with using metals as (contact) electrodes and interconnections. Gold has an excellent conductivity and a work function around 5eV which is suitable for many organic semiconductors, e.g. pentacene where the holes are easily injected from gold contact into pentacene because the ionization energy (corresponding to HOMO level)

of pentacene is very close to 5eV. Carbon was also tested as alternative source and drain electrodes and it gave similar results to gold electrodes, but the former were not as reproducible as the latter. Carbon source and drain electrodes could be used in bottom-contact configuration, whereas gold electrodes, even if cleaned with oxygen plasma, generally produced either lower performances devices or devices that did not operate at all. Interestingly, aluminum electrodes cannot provide active devices, despite the fact that aluminum has a lower work function than gold and hence should be more suitable for electron injection into electron transporters. This might be due to the oxidation of aluminum which creates an insulating layer of aluminum oxide. Another explanation in Al/DP-NTCDI system is that the vacuum level in the organic semiconductor side of the interface of Al/DP-NTCDI moves upwards by −0.2eV, which was attributed to charge transfer from Al to DP-NTCDI, and thus forming an interface dipole. As a result, the electron injection barrier is even increased.[2] Recently, copper was also introduced to the OFETs fabrication and used as contact electrodes. Despite the lower work function (4.65eV) and thus larger holes injection barrier compared to Au, the resulting contact resistances are smaller than those with Au contact.[106] This might be due to the oxidation of Cu at metal/organic interface.[107, 108]

However, the fully organic transistors require electrodes and interconnections also of organic materials, and this meets the solution-based printing for mass production, in particular for the flexible and transparent organic products. Generally, the organic materials could be used as electrode (S/D contact electrodes and gate electrode) and interconnection are conducting polymers. Typical materials are poly (3,4-ethylenedioxythiophene) PEDOT:PSS,[95, 109] polyaniline (PANI),[110] polypyrrole (PPy) as well as graphite-based and Ag/Cu-epoxy inks. In the work of Makela *et al.*,[111] all polymer OFETs were fabricated by roll-to-roll printing with using PANI and PEDOT:PSS as source/drain contact electrodes and gate electrode, respectively. However, due to the limitations of resolution (and/or contact size) and susceptivity to air and humidity, the "off" current is very large and thus the dynamic spanning is narrow. Kang *et al.* reported that the pentacene OFETs using three electrodes (S/D/G) of conducting PEDOT exhibited nearly identical performances to those by using Au electrodes.[112] Gelinck *et al.* had applied PANI as electrodes and interconnections to fabricate all-organic (with OSCs of pentacene, polythienylenevinylene and P3HT) integrated circuits.[113] The sheet resistance after processing was about 1-2kΩ/square, the inverters showed voltage amplification at moderate biases and the seven-stage ring oscillators switching frequencies of a few kHz were also obtained.

■ Organic substrate

One of important factor to achieve all-organic electronics is the substrate. Differing from the conventional silicon MOSFETs, in which the silicon substrate not only serves as mechanical support but also is a basis (bulk) for the device or circuit fabrication, in organic devices the substrate is mostly applied as a mechanical support on which the elements of organic devices are deposited, even thought the substrate surface quality may also affect the resulting devices performances.[46, 104] The thin-film structure of OFETs allows the fabrication of electronic circuits on a variety of substrates, such as silicon, glass, polyimide, polyethylene naphthalate (PEN), polyethylene terephthalate (PET) and polycarbonate, depending on the specific application. For example, backlit liquid crystal displays require clear, transparent substrates, such as glass, PEN or PET. Light emitting and reflective displays allow the use of opaque (or not fully transparent) substrates, such as silicon or polyimide. Flexible electronics, conformable image sensors, and foldable displays call for the mechanical flexibility provided by polymeric film or steel foil. The commercial products targeting low-cost, large-volume applications may require the use of particularly inexpensive substrates, such as PEN, PET even paper.[114] The use of plastic-based substrates, coupled with recent developments in solution-based technologies (in particular the printing over large surface), enables the possibility of mass-production and low-cost processing by

use of roll-to-roll processing. For more details on flexible polymeric substrates can refer to ref.,[1] chapter 7 "*Advanced Flexible Polymeric Substrates*". Very recently, active organic circuits printing on the banknotes for the purpose of anti-counterfeiting have also reported.[115] The large variety of substrates for organic electronics will open the door for broader applications.

■ Organic passivation layer

In the conventional silicon-based IC fabrication, passivation is a necessary step. The passivation layer is usually used as isolating layer for further integration or encapsulation. For organic devices and organic circuits, the passivation layers have another important purpose that is to protect the active organic film from degradation due to the presence of air (oxygen), humidity and other chemical reaction influences, especially for n-type conducting devices. The passivation layer will affect the properties of this open surface, e.g. in bottom-gate OFETs, so attentions should be paid to passivation process and passivation material processing.

Sputtered SiN and polymers such as poly (vinyl acetate) (PVA) and polyvinylphenol are typical passivation materials. Tsukagoshi *et al.* have successfully applied poly-***para***-xylylene film as passivation layer for their pentacene OFETs.[116] And then, Han *et al.* investigated the degradation of pentacene OFETs with comparing unpassivated and polyvinylalcohol and photosensitive acryl layers passivated devices.[117] It was found that the lifetime of half-current degradation is around 11000 hours in ambient air. Meanwhile, the passivation causes a different mechanism responsible for the threshold voltage degradation; the increased absolute values of V_T with time in the unpassivated case is due to the presence of H_2O whereas the decreased values of V_T with time in the passivated case is because of oxygen. The same study was conducted by Jung et al. by using tetratetracontane (n-$C_{44}H_{90}$) as passivation layer for pentacene OFETs. The mobility of passivated OFETs was only degraded from 0.143 cm^2/Vs to 0.12 cm^2/Vs after 50 days exposure to air. However the unpassivated OFETs lost the functionality in 5 days of exposure to ambient condition, the moisture was attributed to as a main reason for such degradation. Lee *et al.* found that the conventional PVA passivation layer is not compatible with the PEDOT:PSS inkjet processing and hence proposed a PVA/PVA/photoacryl (PA) multi-passivation system for their pentacene OFETs.[118] Wu *et al.* also tested the PVA passivation for pentacene OFETs, the passivated devices could withstand up to 2500 bending cycles of 80°.[119] More recently, Hyung *et al.* used polyimide (PI) instead of common PVA passivation layer for their pentacene OFETs, the half-life time of passivated devices is extended to 360h with respect to 24h of the unpassivated ones.[120]

With all of these contributions, more and more all-organic electronics emerge in the literature[36, 95, 109, 110, 113, 121-126] which will rapidly push the all-organic electronic products toward the consumer market in the near future.

1.5 CONCLUSIONS

In this chapter, the carrier transport in organic semiconductors in comparison with that in the classical inorganic material (silicon) has first been presented. The weak van der Waals forces interacting between molecules, the large band-gap, the disorders and the impurities give rise to a complex and low-efficiency carrier transport. And then, one deals with the principal parameters related to the performances of organic semiconductors: mobility and conductivity. There is a specific relationship between them but for application of organic transistors, they are sometimes a pair of contradictions. Next, one discusses the main organic semiconductors: small molecular, polymeric and n-type semiconductors; and some typical organic semiconductors are discussed. In the end, the other (organic) materials used for OFETs' fabrication are also analyzed: organic

dielectrics, organic electrodes and interconnections, organic substrates as well as organic passivation layers. I believe that the future progresses made in material science will significantly promote the performances of organic devices and open up a broader space for the development of organic electronics.

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Chapter 2
Organic field-effect transistors (OFETs)

Because the thin film of organic material is generally used in organic transistors instead of the bulk semiconductor as in the classical silicon MOSFETs, the organic transistors are usually called organic thin-film transistors (OTFTs). Due to the unipolar conduction as in the conventional field-effect transistors, they are also called organic field-effect transistors (OFETs). The term of OFETs will be applied throughout this thesis.

As usual, a brief introduction of Si MOSFETs is given to compare with the organic transistors.

2.1 STRUCTURE AND OPERATION OF OFETS

2.1.1 SILICON MOSFETS

■ Structure of Si MOSFETs

Fig. 2.1 shows the schematic diagram of an n-type MOSFET.

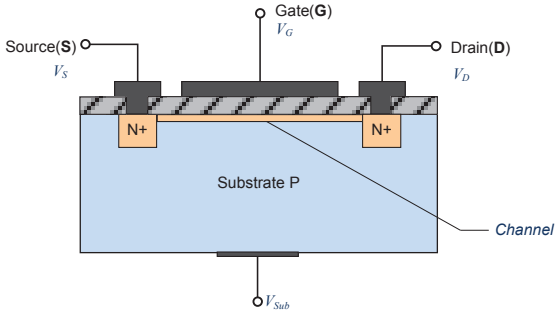

Figure 2.1 | Cross section schematic of an n-type MOSFET fabricated on a p-type doped substrate. The source and drain contacting regions are heavily n-type doped, which connect the same conducting type of inversion layer (channel) in the substrate and in close vicinity of the Si/dielectric interface. Over the substrate, a gate insulator is formed, often by oxidation of silicon or others materials (e.g. High *k*). Finally, an interconnection layer including S/D and gate electrodes is made, usually by deposition of metal. Therefore, such a structure is called as Metal-

Fig. 2.2 shows the band diagram of that structure of metal-oxide-semiconductor (MOS) without contact.

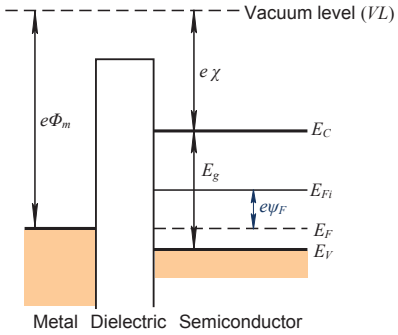

Figure 2.2 | Band diagram of the transistor shown above at zero gate bias. In this case, the bands in semiconductor are flat throughout the subtract thickness. The Fermi level is shifted to close the valence band due to the p-type doping, and its value equals to the Fermi level of the gate electrode (metal). The difference of Fermi level from its intrinsic value is defined as a potential ψ_F, which will be used for further discussion.

■ Operating mode of Si MOSFETs

For that n-type MOSFET shown in Fig. 2.1, its operation could be divided into 3 modes, depending on the applied gate bias on the gate electrode, V_G. Here the source electrode and the substrate are connected to the ground, i.e. V_S=V_{sub}=0V.

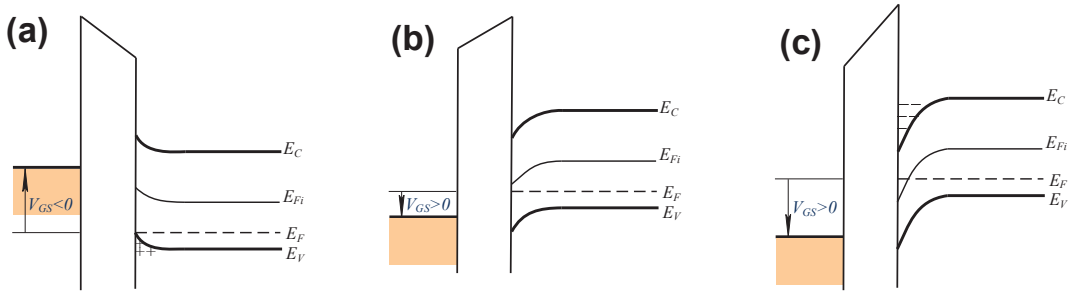

Figure 2.3 | Band diagrams of the three operating modes of above n-type MOSFET: (a) accumulation, (b) depletion, (c) inversion.

■■ **Accumulation mode (V_G<0V):** If a negative V_G is applied, the gate electrical field attracts the majority carriers (here holes for the p-type doped silicon bulk) from the substrate bulk to the semiconductor/oxide interface. Hence the concentration of hole is significantly increased and the bands of Si bulk are bent close to the gate dielectric, as shown in Fig. 2.3a.

■■ **Depletion mode (0V<V_G<V_T):** With a small positive V_G is applied(less than the threshold voltage, V_T), the gate electrical field pushes the holes away from the Si/oxide interface into the substrate bulk, thus leaving the fixed negative charges (electrons) near the interface and forming a space charge region. This region depletes the holes, and this mode is called depletion mode, cf. Fig. 2.3b. The surface potential ψ_s is smaller than the difference of Fermi level to its intrinsic level ψ_F, i.e. $0<\psi_s<\psi_F$ and the concentration of electrons n_s is much less than that of holes at thermal equilibrium p_0, namely $n_s<<p_s<<p_0$.

■■ **Inversion mode (0V<V_T<V_G):** With a positive V_G greater than V_T, the band bending in the space charge region will be significant and the Fermi level moves towards the conduction band so that a large number of free electrons are induced. Here one defines the threshold voltage V_T, at which the concentration of the induced negative charges is equal to the concentration of holes in the intrinsic doped Si bulk. This case corresponds to the difference of the Fermi level and its intrinsic level, but their relative position is opposite, cf. Fig.2.3c. Increasing V_G further, a narrow region in the close vicinity of the Si/oxide interface is rich in electrons, this region is called inversion layer. This layer is located between the source and drain electrodes where the contacting well is heavily n-type doped. Applying a drain voltage, it will directly cause a current between the S/D along the narrow inversion layer (channel).

Sometimes, the inversion mode is identified as weak inversion and strong inversion, the borderline is the threshold voltage. In weak inversion ($V_G<V_T$), $\psi_s>\psi_F$ but $\psi_s<2\psi_F$ (corresponding to V_T), namely $\psi_F<\psi_s<2\psi_F$. Hence the inversion charges Q_i is less than the depletion charges Q_D, i.e. $Q_i<Q_D$. On the contrary, in strong inversion ($V_G>V_T$) $\psi_s>2\psi_F$ and $Q_i>Q_D$.

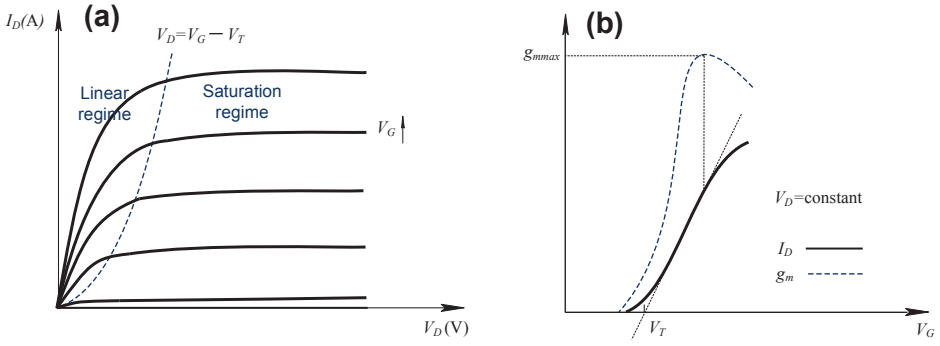

Figure 2.4 | (a) Typical output characteristics of above MOSFET at various gate voltages. The blue dashed line separates the linear and saturation regime. At small drain voltages, the drain current increases linearly with drain voltage. As the drain voltage increases further and attains the borderline (V_G-V_T), the drain current saturates. (b) Typical transfer characteristics of that n-type Si MOSFET in linear regime, where the drain voltage is small and kept constant. At higher gate voltages, the transconductance (blue dashed line) reaches its maximum and attenuated with the further increased gate electrical field. This feature is usually used to extract the threshold voltage.

Due to the drain voltage affects the uniformity of the channel potentials from source side to the drain side, hence the channel conduction could also be divided to two regimes:

■■ **Linear regime (V_D<(V_G−V_T)):** With a very small V_D, the channel is nearly uniform. The channel could be regarded as a resistance whose conductance is controlled by the gate voltage. Hence the transistor works as a linear resistance and this operation is also called ohmic regime. In this case, the transfer characteristics I_D-V_G read:

$$I_{DS} = \frac{W}{L}\mu C_i (V_G - V_T - \frac{V_D}{2})V_D \tag{2.1}$$

where W and L are the channel width and length, respectively. C_i is the unit area capacitance of the gate dielectric, μ is the effective mobility.

■■ **Saturation regime (V_D>(V_G−V_T)):** As V_D is increased, the channel is not uniform. On the side of drain electrode, the effective channel potential difference falls to V_G−V_D. With more increase of V_D, that effective potential difference arrives a key point of $(V_G-V_D)=V_T$ or $V_{Dsat}=(V_G-V_T)$, at which the channel near the drain electrode is pinched off. Further increasing V_D, the pinch-off will take place towards the source side. The potential difference at the pinch-off point remains the same value of V_{Dsat}, hence the number of carriers arriving at this point and thus the current flowing from the source to drain remains also the same value of:

$$I_{Dsat} = \frac{W}{2L}\mu C_i (V_G - V_T)^2 \tag{2.2}$$

In this case, the drain current saturates to I_{Dsat}. The two regimes are shown in Fig. 2.4.

2.1.2 Organic field-effect transistors (OFETS)

■ **Structure of OFETs**

A typical structure of OFETs is shown in Fig. 2.5. Compared to Si MOSFETs, one can find some differences in OFETs: **1.**) The channel is not located in the bulk of substrate but rather in the thin film of organic semiconductor. Hence the substrate serves mostly as a mechanical support (sometimes as gate electrode, e.g. bottom gate), and it is not necessary being semiconductors and could be glass, plastic film or paper. **2.**) The source and drain electrodes, often in metal, are directly contacted to the organic film without highly doped wells, forming Schottky junctions with the oppositely doped substrate. Such a configuration significantly decreases the access resistance and efficiently blocks the channel current at OFF state. For OFETs, the access resistance usually is very high (it will be discussed later), and the switch-off relies on the low conductivity of the intrinsic OSCs. **3.**) The OSCs are generally intrinsic and made by deposition.

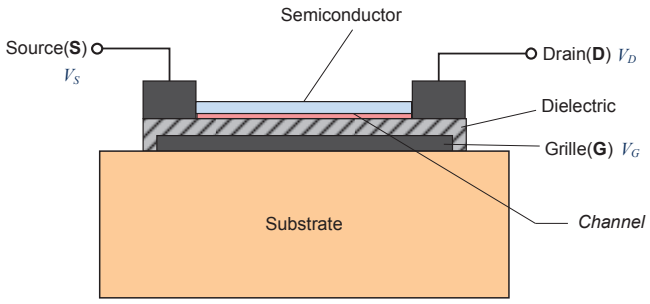

Figure 2.5 | Section schematic of an organic thin-film transistor (OTFT). Note that the channel is not located in subtract but rather in the very thin organic film.

Based on the different architectures, there are two configurations for the gate electrode as well as for the source/drain electrodes. So we have the top-gate (TG)/bottom-gate (BG) and top-contact (TC)/bottom-contact (BC) configurations, as seen in Fig. 2.6.

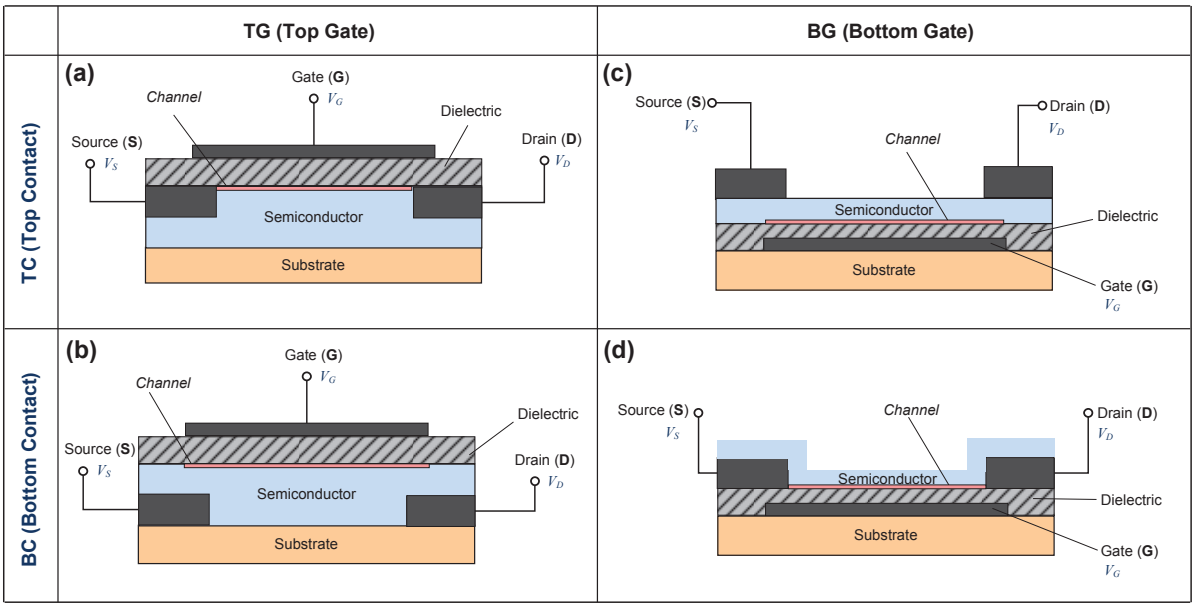

Figure 2.6 | Section schematic of four configurations of organic transistors. (a) and (b) are top-gate (TG) configured, with top-contact(TC) and bottom-contact (BC) configured source and drain electrodes, respectively. (c) and (d) are bottom-gate (BG) configured, with TC and BC source/drain electrodes, respectively.

The choice of architecture has a significant effect on the OFETs' electrical properties. With regard to TG/BG configuration, if the substrate is the BG the OFETs with such a common gate electrode will be easy to fabricate but it is not suitable for a practical circuit which necessitates separate gate electrode for each transistor. For TG devices, because the gate insulator is deposited over the OSC film, the insulator should be easy to be dissolved in the solvents and does not degrade the nether OSC film. Therefore, the TG OFETs often suffer from the OSC/dielectric interface roughness and high "off" current, which may arise from the oxygen doping during the deposition of insulator on the OSC film. Another issue on TG devices is the misalignment: the top-gate should accurately and completely cover the entire channel length defined by S/D. If a misalignment or ungated gap in S/D occurs, additional access resistance will be introduced, resulting in higher contact resistance.

With regard to TC/BC configuration, BC configuration is more desired for reducing fabrication complexity but BC devices generally exhibit lower performances than TC counterparts, e.g. lower mobility and higher contact resistance. A well-known explanation is that, during the OSC deposition, the self organization (on the surface of insulator or substrate) of organic molecules is disrupted by the presence of the source and drain electrodes, hence very small size grains are formed in the vicinity of the contact.[10] A large number of traps existing in this small grain region are responsible for the smaller mobility and higher contact resistance in BC OFETs. This issue will be addressed in detail later. On the other hand, the TC OFETs require applying shadow mask which increases the cost and the technological complexity. With the new types of shadow masks, such as SAMs and new metal masks, such difficulties are being much ameliorated.

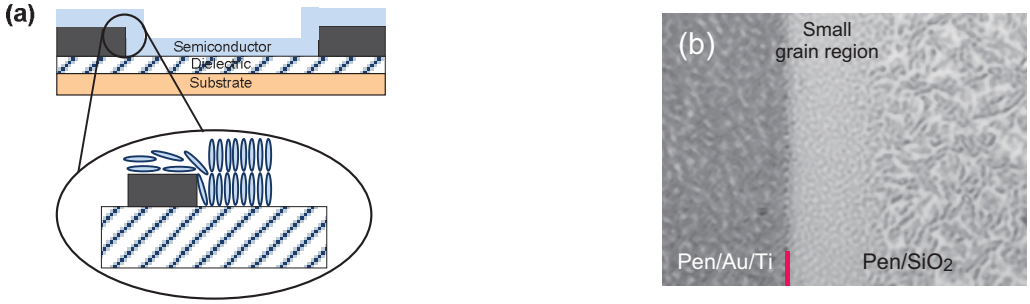

Figure 2.7 | (a) Illustration of the self-organization process during the organic semiconductor deposition. Due to the presence of contacts, such an original self-organization process of molecules is disrupted, resulting in small grain at the contact edges, as shown in (b) (after Xu 2010[6]).

There exist also two designations: coplanar or staggered structure. The coplanar one is that the S/D contacts and the channel are on the same side of OSC film, e.g., BC-TG and TC-BG (cf. Fig. 2.6a and b). The staggered one is that the S/D contacts and the channel are on the opposite side of OSC film, e.g., BC-BG (cf. Fig. 2.6 c). In this case, the carriers have to traverse the entire thickness of organic film. The access resistance is thus higher and stronger dependent on the gate voltage as compared to the coplanar transistors.[3]

■ Operating mode of OFETs

Organic transistors exhibit similar field-effect behaviors as the conventional silicon MOSFETs, including output and transfer characteristics. However, due to the absence of the doped bulk substrate, the depletion and thus the inversion mode are lost in OFETs. Increasing the gate voltage, the charges will be injected from source and/or drain into the organic film, forming a conducting channel next to the gate dielectric. Hence only the accumulation mode remains. For the non-accumulation mode, i.e. "OFF" state, the switch-off of the channel is realized by the natural low conductivity of intrinsic OSCs since the reverse p-n junctions in silicon MOSFETs is absent here. At small drain voltage, OFETs work in linear (ohmic) regime and thus, the channel is nearly uniform and can be regarded as a linear resistance governed by the gate voltage. As the drain voltage is much increased, similar "pinch-off" behavior on drain side alike in Si MOSFETs occurs, corresponding to saturation regime.

Because the holes are easier to be injected from contacts into organic semiconductors relative to electrons, most of OFETs are p-type transistors. Negative voltages are applied to gate and drain electrodes with respect to the common and grounded source voltage.

2.2 PRINCIPAL PARAMETERS

■ Mobility

The mobility discussed in the first chapter is for organic semiconductors. Several kinds of scattering in the bulk of organic semiconductors (e.g., lattice and phonon scattering, ionized and neutral impurity scattering), significantly diminish mobility as reported by Mathiessen's rule:[11]

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \ldots\ldots \qquad (2.3)$$

The lowest one will dominate the overall mobility.

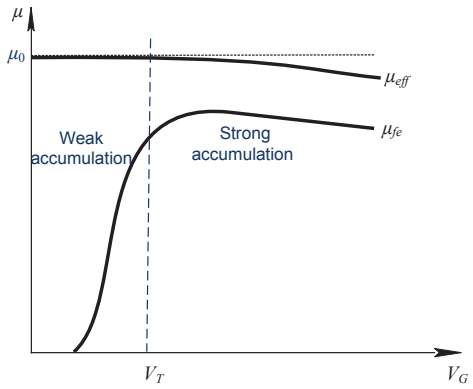

Figure 2.8 | Illustration of three mobilities in organic transistors. The effective mobility and the field-effect mobility are decreased with V_G at higher gate voltages. At low gate voltage or gate electrical field, the effective mobility approaches its upper bound: low-field mobility. Hence the low-field mobility is an intrinsic mobility in transistors. Note that the filed-effect mobility is significantly reduced at high gate voltages.

Compared to the microscopic mobility in OSC, the carrier mobility in OFETs is a macroscopic and more extrinsic parameter. i) Because the carriers are confined in a narrow region close to the gate dielectric, the fixed charges in the gate dielectric and/or in the OSC bulk will also give scattering by Coulomb forces. ii) The surface roughness of the OSC/dielectric interface will also introduce scattering and reduce the mobility. iii) The electronic traps distributed in the gate dielectric and/or in the OSC bulk significantly affect the carrier

transport and thus decrease the OFETs' mobility. That's why the mobility is quite different in the OFETs having diverse grain size, architecture (e.g. between TC/BC).

Here, one should distinguish various definitions of mobility in OFETs. ***Low-field mobility***, μ_0 is a nearly intrinsic mobility for the organic transistors and hence, it is independent of extrinsic effects such as contact resistance and gate-voltage dependent mobility. ***Effective mobility***, μ_{eff} usually measured at small drain voltages, is an apparent or average mobility for all carriers in the channel. It is affected by several factors, e.g., surface roughness scattering, phonon scattering and contact resistance, and its upper limit is μ_0. ***Field-effect mobility***, μ_{fe} is deduced from the transconductance of transistors and is normally lower than μ_{eff} and also much lower than μ_0. A simple illustration is shown in Fig. 2.8 and an explicit discussion will be done in the next chapter.

Gate-voltage dependent mobility

The literature has reported that the carrier mobility in OFETs is enhanced by gate voltage, following a power-law as: [12, 13]

$$\mu = k(V_G - V_T)^{\alpha} \tag{2.4}$$

where k and α are constants. This relation was found to be generally valid in the OFETs with polycrystalline and amorphous OSCs. This is due to the fact that in disordered semiconductors, a large number of traps lied in the OSC bulk (and/or in the gate insulator) localize the charge carriers; the transport is by hopping from one site to next one where it exists a hopping barrier. At a small gate voltage, the hopping barrier is quite large so that a considerable portion of charge carriers are trapped and cannot contribute to the current. Hence the apparent mobility is small, cf. Fig.2.9. At higher gate voltages, the Fermi level sweeps through the trap states, the deeper ones are nearly filled and the next induced carriers can move more freely, manifesting as a higher mobility.

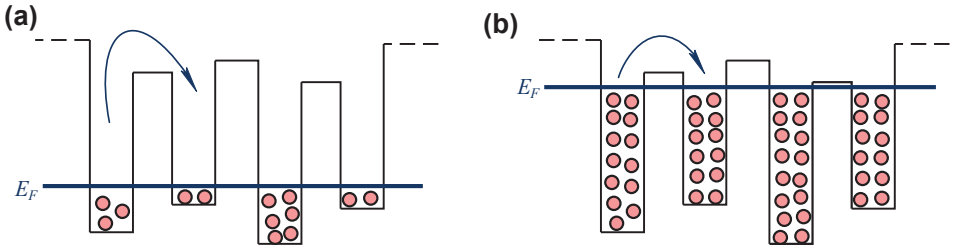

Figure 2.9 | Charge hopping in disordered system. (a) At small gate voltage, the low charge density corresponds to a low Fermi level, the hopping barrier is large. (b) As gate voltage is increased, the Fermi level sweeps over the deep trap states, filling the deep traps. The hopping barrier is getting smaller, thus the apparent mobility increases.

This inference is confirmed by the smaller activation energy for mobility at higher gate voltages.

Similar feature was also studied by Podzorov *et al.*[14] in the Hall Effect measurement of single-crystal rubrene OFETs. According to the MTR model:

$$\mu_{eff} \equiv \frac{\sigma}{qn} = \mu_0 \frac{\tau}{\tau + \tau_{tr}} \tag{2.5}$$

where σ is the channel conductivity, q is the electron charge and n is the charge density in the channel. μ_0 here characterizes the trap-free mobility, τ and τ_{tr} represents the average traveling time from one state to next one and the trapped time, respectively. This effect is alternatively expressed as:

$$n_{eff} = n \frac{\tau}{\tau + \tau_{tr}} \tag{2.6}$$

where n_{eff} is the mobile charge density relative to n. Owing to the presence of traps, only a certain number of mobile charge carriers contribute to the current. However, such a relative trap-

ping effect is changed by shifting the Fermi level. As the deep traps are filled, more mobile charge carriers are induced or the overall carriers move faster, the apparent mobility increases.

In the works of Horowitz,[15, 16] the apparent mobility in the OFETs with polycrystalline OSCs was found to be also dependent on the grain size. Mobility increases with grain size when the grain size is very small, and the mobility shows a strong gate-voltage enhancement[17] and a clear thermal activation behavior.[16] However mobility tends to saturate with grain size as large grains[18] or a single grain are formed,[17, 19] the gate-voltage and thermal activation of mobility become very slight. This is because most of defects are confined in grain boundaries, and the charge carriers will be much localized by the traps at grain boundaries but could move more freely within grains where the trap density and trap depth are much lower than those at grain boundaries. So the polycrystalline OSC medium could be divided into high (grains) and low (grain boundaries) conductivity region, and they are connected alternately and in series. Suppose the size of grains (L_G) is much larger than that of the grain boundaries (L_{GB}), the effective mobility of the polycrystalline medium (μ) could be read as:

$$\frac{L_G + L_{GB}}{\mu} = \frac{L_G}{\mu_G} + \frac{L_{GB}}{\mu_{GB}} \tag{2.7}$$

or

$$\frac{\mu}{\mu_G} = \frac{L_G + L_{GB}}{L_G + L_{GB}\left(\mu_G / \mu_{GB}\right)} \tag{2.8}$$

where μ_G and μ_{GB} are the mobility in grains and at grain boundaries, respectively. Eq. 2.8 describes the ratio of overall effective mobility to that in grains with respect to different L_G if L_{GB} is assumed constant. A linear increase of μ/μ_G with L_G can be found at small L_G, and then it saturates to 1, which means the overall effective mobility approaches to that in grains.[15]

Therefore, this gate-voltage enhancement of mobility is less pronounced in the OFETs with better quality OSCs and even disappears in the OFETs with single-crystal OSCs, and instead the mobility decreases with gate voltage due to the more intense scattering induced by the higher density of carriers. Actually, intrinsic carrier mobility, e.g. Hall Effect mobility, doesn't depend on the gate voltage.[20]

■ Threshold voltage

Threshold voltage is a crucial parameter for the other parameter evaluation,[21] such as mobility, contact resistance. For instance, the charge approximation of $C_i(V_G - V_T)$ is widely used for mobility analysis, especially in the Hall Effect measurements.[22-24] In Si MOSFETs, threshold voltage separates the weak and strong inversion from the Fermi level shifts, or more simply separates the on/off state of transistors. Its value is determined by the doping dose and the substrate-source voltage as(cf. Ref.[25] P440):

$$V_T = 2\psi_F + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_F)}}{C_i} \tag{2.9}$$

where ε_s is the semiconductor permittivity and N_A is the acceptor doping level for a n-type MOSFET.

However in organic transistors, its conventional meaning is lost since OFETs are thin-film transistors with non-doped OSCs. In an ideal situation (zero difference of the gate work function and the Fermi level of OSC, zero charge injection barrier), the threshold voltage is zero because the greater gate voltages immediately accumulate charge carriers and increases the OSCs conductivity, but at zero gate voltage the OSCs conductivity returns to their natural low value which is desired to block the channel. Due to the large number of traps distributed in OFETs and the presence of charge injection barrier, the threshold voltage is significantly shifted, particularly in polymer OFETs. Well control its values is important for the applications where high uniformity of electrical characteristics from device-to-device is required, such as display and logic circuit.

The above discussed threshold voltage is actually a charge threshold. In current OFETs community, there exists a mobility threshold voltage, at which the mobile charge density is greater than that of the trapped charge density, due to the charge trapping in organic transistors.[26, 27]

■ Contact resistance

In Si MOSFETs, the heavily doped contact regions which connect the same conduction type of the inversion channel give very low access resistance or contact resistance. In OFETs, the charge carriers are injected from contacts into OSCs through a Schottky junction where an injection barrier increases the contact resistance, since higher voltage (or potential drop) is needed. Moreover, in the staggered OFETs the carriers must traverse the organic film where the bulk conductivity is very low, and in the coplanar OFETs the carriers must flow across the contact/OSC region where high density of traps reside in, the two contributions also increase contact resistance.

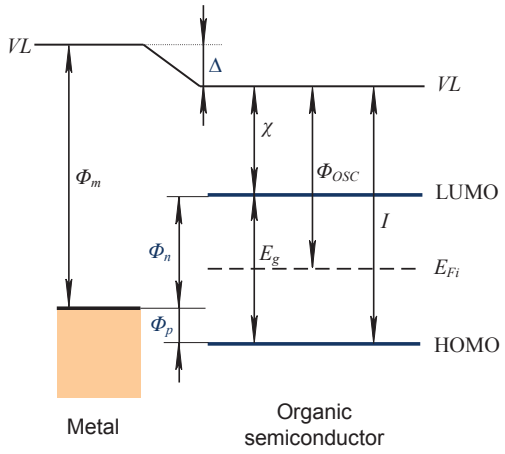

Figure 2.10 | Band diagram of a structure of contact (metal) and organic semiconductor. Note the interface dipole Δ which alters the hole injection barrier Φ_p and the electron iniection barrier Φ_n.

■■ Interfacial dipole impact on contact resistance

The classical Schottky-Mott rule and thus the energy level alignment at the contact/OSC interface are not always held as the thin-film organic semiconductor deposits on the pre-patterned contacts (often in metal) or the contact metal deposits on the OSC layer. The interfacial dipole alters the original injection barrier.[4, 5, 8, 28]

In the pioneer work of Ishii *et al.*,[5] they explained two different definitions of vacuum level (*VL*) and that is the source of much confusion in analyzing the surface dipole. When an isolated electron is at rest in vacuum, it is referred to at the *VL*. As an electron at rest and at infinite distance from the system, the *VL* is denoted as *VL*(∞) and that is often used as reference. However, the *VL* of a solid used for measuring ionization energy, electron affinity and work function is the energy of an electron at rest just outside the solid, and it is affected by the solid potential. This surface *VL* is often denoted as *VL*(s).

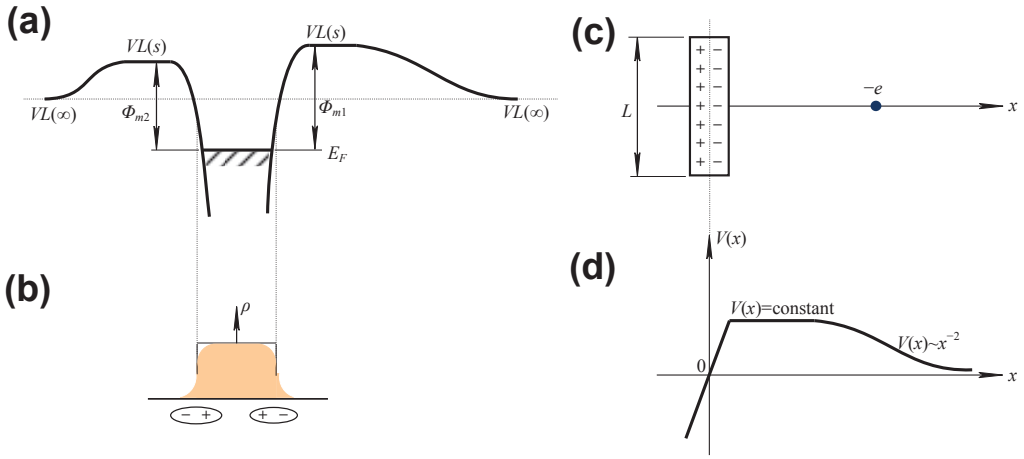

Figure 2.11 | (a) Potential surface for an electron in and out of a metal crystal, where E_F is the Fermi level, *VL*(s) and *VL*(∞) are the vacuum level at surfaces and at infinite distance, respectively. Φ_{m1} and Φ_{m2} are the work function at different crystal surface. (b) Electron density in the metal with tailing at the surface to form a surface dipole layer. (c) Electron and dipole layer with a specific extension *L* with the distance *x* between them. (d) Potential energy of the electron by the dipole layer in (c). (remade and after Ishii 1999[5])

The two *VL*s are actually not identical. The evidence of the dependence of the work function on various surface of single-crystal tungsten indicates the energy difference for an electron just outside the surface or *VL*(s), as shown in Fig. 2.11a.

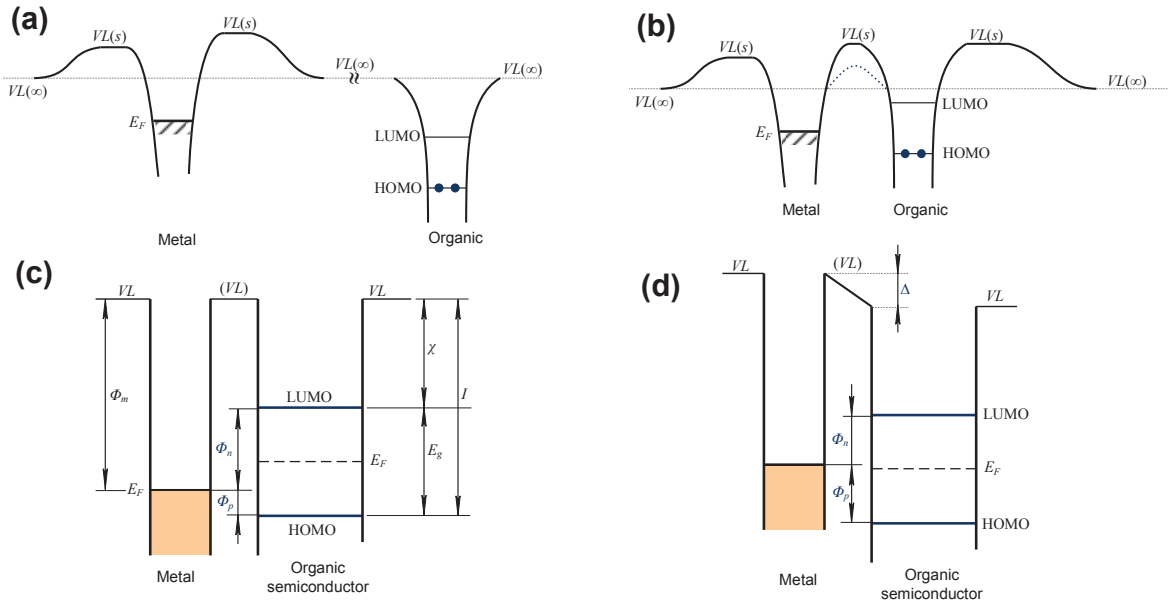

Figure 2.12 | (a) Electronic structure of a metal and organic material at infinite distance. (b) Contact of metal and a thin organic layer, in which the energy levels of organic layer is shifted upwards to sharing the common *VL*(s). (c) and (d) are the simplification of (b) without and with a interface dipole. (remade after Ishii 1999[5])

Hence the Fermi level is a common level inside solid. The difference between $VL(\infty)$ and $VL(s)$ is actually resulting from the surface dipole layer formed by tailing of electron cloud at surface, as shown by the electron density distribution in Fig. 2.11b. The tailing of negatively charged electron cloud into vacuum causes the vacuum side negative charged, whereas the bulk side is positively charged due to the lack of electrons. When an electron is at distance x from a dipole layer which extends finitely with a characteristic length L, cf. Fig. 2.11d, the potential energy $V(x)$ induced by such a dipole layer is shown in Fig. 2.11c. If $x<<L$, the dipole layer can be seen as infinitely extended, the $V(x)$ on both sides is abruptly changed and independent of x. If $x>>L$, the dipole layer could be regarded as a point dipole and the $V(x)$ decays as x^{-2}. The dipole layer explains

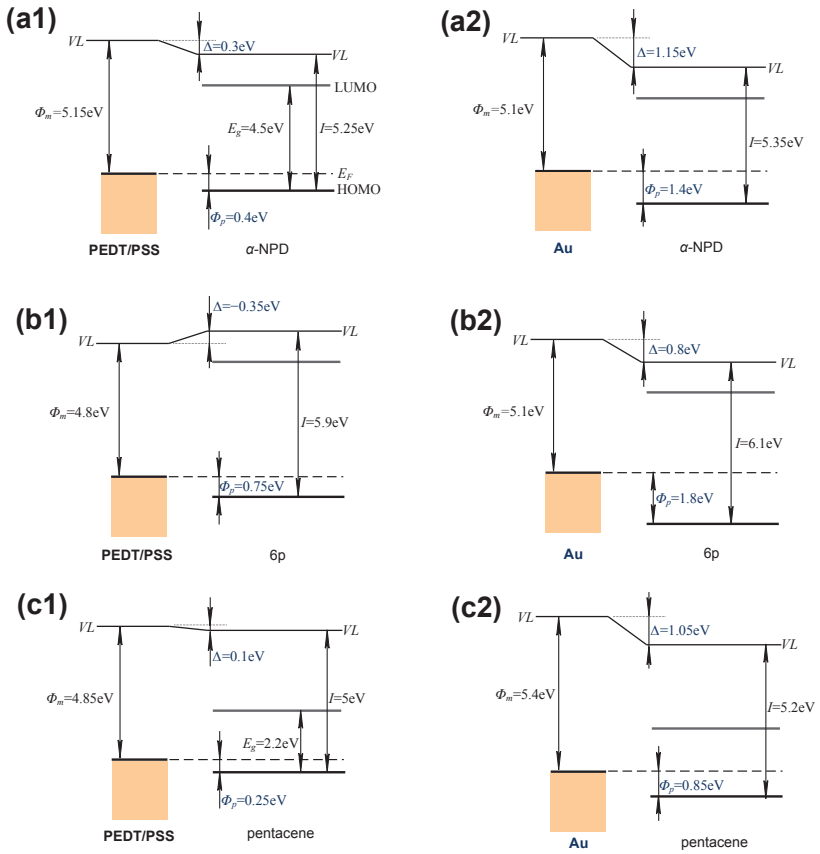

Figure 2.13 | Electronic structure of PEDT/PSS (left side) or Au (right side) deposited on α–NPD (a), 6p(b) and pentacene(c), respectively. Compared to Au, the interface dipole with conducting polymer results in much smaller hole injection barriers. (remade after Koch 2003[8])

the different work functions at different surface, and if the electron is far away from the dipole layer, the effects of dipole layer vanish and its energy will return to its intrinsic values, which corresponds to $VL(\infty)$.

The interface dipole is formed between the interface of two different types of solid by either contacting or deposition, often at the organic/organic and metal/organic interface. Fig. 2.12a shows the energy diagrams of a metal and organic metal as they are very far away. Their energy levels are aligned with sharing a common $VL(\infty)$. However, if they are contacted together *without rearrangement of electric charges*, the organic layer will be within the surface dipole of the metal $VL(s)$, hence its energy levels are raised upwards in an *extremely narrow interfacial gap* to attain a common $VL(s)$, and the common $VL(\infty)$ reference becomes no longer important, as seen in Fig. 2.12b. Simply seeing, the energy diagram is described with a uniform VL as shown in Fig. 2.12c. However, sometimes an additional interface dipole is indeed created due to such as charge transfer, redistribution of electron cloud, interfacial chemical reaction and other types of rearrangement of electronic charges.[5] Hence the injection barriers of electrons and holes defined in Fig. 2.12c will be changed with a shift of Δ, as seen in Fig. 2.12d. The interface dipole Δ is quite large in the range of 0.5-1eV for most of metal-organic semiconductor interfaces.

$$\begin{aligned} \Phi_p &= I - \Phi_m - \Delta \\ \Phi_n &= \Phi_m - \chi = E_g - \Phi_p \end{aligned} \tag{2.10}$$

In the work of Koch and Kahn,[8] they also found that the interface dipole is due to the lowering of the metal work function by the absorbed molecules.[5] Because the work function of a metal comprises both bulk and surface-dipole contribution, the latter corresponds to the tail of electrons spilling out from the metal surface into the vacuum. This surface-dipole contribution is always substantially modified by the presence of an absorbate. If the absorbate is large, such as in conjugated organic molecules, the repulsion between the molecule electrons and the metal surface electrons leads to a compression of the electron tail, thus resulting in a lowering of the metal work function by revealing an abrupt downward shift of the vacuum level from the metal to the organic film at the interface. Upon this consideration, they used a conducting polymer PEDT/PSS to investigate the interface dipole. Compared to Au, the PEDT/PSS is made of closed-shell molecules and has much fewer free electrons. The experimental results indicated that the formed interface dipoles is significantly reduced, from 1.15eV to 0.3eV [with N,N'-bis-(1-naphthyl)-N,N'-diphenyl1-1,1-biphenyl1-4,4'-diamine (α-NPD)], 0.8eV to −0.35eV [with *para*-sexiphenyl(6P)] and 1.05eV to 0.1eV (with pentacene), by using PEDT/PSS instead of Au, respectively. Hence the resulted hole injection barrier is reduced from 1.4eV to 0.4eV (with α-NPD), 1.8eV to 0.75eV (with 6P) and 0.85eV to 0.25eV (with pentacene), as seen in Fig. 2.13. Note that the negative value means that the vacuum level rises from the polymer electrode to the molecular film, cf. Fig. 2.13b1.

Such a high Φ_p with Au is resulting from the significantly shift of work function, in which an important contribution is from the change of the metal surface dipole. It is due to the fact that the electron density tailing from the free surface into vacuum is pushed back into the solid upon absorption, reducing the surface dipole and effectively decreasing the work function of the covered surface.[5] However, with PEDT/PSS where the work function is mainly controlled by the energy levels created by the charge transfer. Such a charge transfer indeed leads to dipoles within the polymer but they have random orientation and

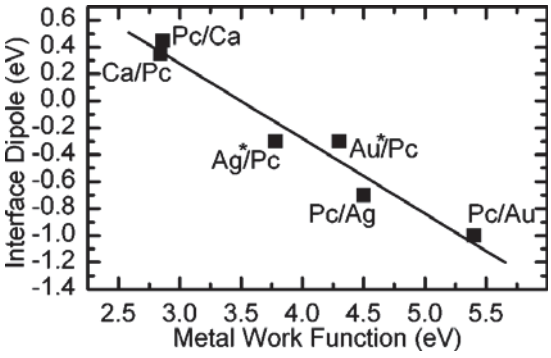

Figure 2.14 | Interface dipole with respect to metal work function. For Au and Ag, a clear asymmetric behavior can be identified, whereas it is not obvious for Ca. Despite those asymmetry, a nearly linear variation is still obtained. (after Watkins 2002[4])

thus cancel each other macroscopically, resulting in much smaller work function shift of PEDT/PSS with respect to Au.

At the same time, Watkins *et al.*[4] examined the interface dipole between the commonly used metals(Au, Ag, Ca) and pentacene by asymmetric deposition order. **i)** As pentacene is deposited on metal surface, a large vacuum level shift is observed when the pentacene thickness is only 2Å, e.g., −0.8eV for Au, −0.6eV for Ag and 0.4eV for Ca. Interestingly, the subsequent deposition has a very slight effect on the *VL* shift. All of these results indicate that the initial change of *VL* is due to the formation of interface dipole layer which is almost completely formed within 8Å pentacene. **ii)** As metal is deposited on pentacene, a significant decrease of metal work function is observed. It is attributed to the metal penetration into the pentacene bulk, forming a mixture of organic and metal thus doping the upper layers. This impact is more pronounced at slower deposition rate since the diffusion of metal in pentacene becomes easier. Therefore, the hole injection barrier is different, e.g., Φ_p=0.5eV for pentacene on Au but Φ_p=1eV for Au on pentacene.

On the basis of the prediction of Tung,[29] which suggests a linear variation of interface dipole with metal work function, the similar linear variation is obtained irrespective of the asymmetric values. One should note that such an asymmetric effect is not clear in Ca and it is due to its reaction with pentacene, the diffusion of metal into organic semiconductors is much less slower compared to noble metals and hence, a fairly pure metal/OSCs interface is formed independent of deposition order.

TC/BC impact on contact resistance

A number of works reported that the contact resistance in BC OFETs is much higher than that in TC devices. Here we summarize the possible explanations. The most widely accepted one is as discussed above that in BC OFETs, due to the presence of contacts the self-organization process of molecules is disrupted[10] and hence, very small grains[30, 31] even voids[32, 33] are formed at the contact edges, resulting in a large number of traps which capture the passing carriers and significantly reduce the carrier mobility in the contact region, manifesting as higher contact resistance.

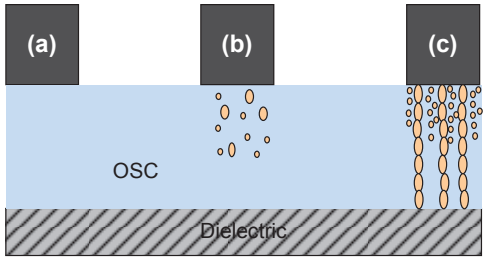

Figure 2.15 | Illustration of metal penetration into organic film. (a) Abrupt interface without penetration, e.g. deposition at very high temperature. (b) With moderate penetration. (c) With very efficient penetration, the metal clusters reach the dielectric surface. (remade after Pesavento 2006[9])

As charge carriers are injected from contacts, the injection barrier is a key factor to determine contact resistance. The different charge injection barrier can explain the non-linear behavior sometimes observed in BC OFETs[34] but cannot account for higher BC contact resistance. However, the injection area in TC OFETs might be much larger, since in TC OFETs there exists a compensation mechanism that the injection area is increased with smaller injection barrier,[34, 35] or the effective injection area is enlarged with increasing the gate voltage, according to the current crowding theory.[3] However, such an area enlarging behavior impossibly occurs in BC OFETs as only a small contact edge contributes to charge injection.

Another factor is the metal penetration into the organic film. As seen in Fig. 2.15, the metal, in particular noble metals, diffuses into the organic bulk, forming clusters of metallic and nonmetallic metal atoms.[36] As the diffusion is expanded, the effective contact area is significantly increased. More importantly, if the metal penetrates the entire organic film (very thin generally) and reaches the dielectric surface where a channel will be created, the access resistance falls down to nearly zero. This feature is also important to explain the gate-voltage dependent contact resistance which will be discussed later.

Staggered/Coplanar impact on contact resistance

In the coplanar configuration, the effective contact area is determined by the contact thickness and the width. Due to the very thin organic film, the contact thickness is small and the contact area is thus very small. On the other hand, in the staggered geometry the contact area depends on the overlap between the gate and source/drain electrode (generally at the level of μm), hence the contact area is much larger than that in the coplanar counterparts.[37] That's also why the bottom-gate and top-contact OFETs exhibit smaller contact resistance than their bottom-contact counterparts. It is widely believed that, in staggered OFETs the overall contact resistance is dominated by the bulk resistance, however in coplanar OFETs the overall contact resistance is dominated by the contribution of a low conductive access region in the immediate vicinity of contacts where a large number of defects and thus charge traps reside in.[30, 32] This could explain the stronger gate-voltage dependence of contact resistance in staggered devices, the bulk dominant resistance strongly relies on the carrier density controlled by the gate voltage.[3] The dominant defect-rich access component in coplanar devices sometimes is characterized a depletion region at negative gate biases, its width is modulated by the gate voltage, resulting in a gate-voltage dependent contact resistance. Note that the variation range with gate voltage in staggered OFETs is much larger than in coplanar transistors.[33]

Gate-voltage dependent contact resistance

Differing from Si MOSFETs in which the access resistance is nearly independent of gate voltage, the contact resistance in OFETs usually exhibits a significant decrease with increasing the gate voltage. This might be due to the carrier transport in the contact region and/or charge injection is significantly affected by the charge density and thus the gate voltage. If the above discussed injection barrier exists, increasing the gate voltage will enhance the charge injection efficiency.[34] Moreover, more induced charges will fill the deep traps in contact regions, especially for BC contacts, facilitating the contact carrier transport.[38] Furthermore, the charge density in the organic bulk is modulated by the gate voltage,[36] also contributing to the gate-voltage dependence.

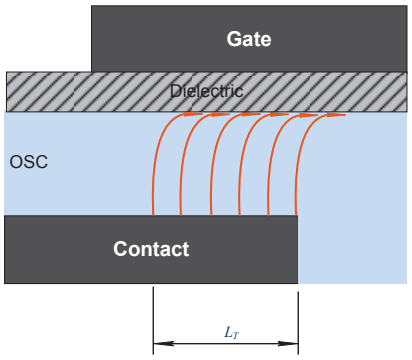

Figure 2.16 | Illustration of the charge injection area modulation by gate voltage. The shift of the injection edge from the contact edge to the contact center is denoted by L_T. (after Richards 2008 [3])

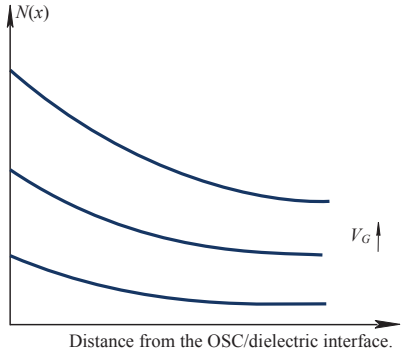

Figure 2.17 | Charge concentration profile in the organic film. The gate voltage increases the charge concentration in the bulk and thus decreases the access resistance of the contact region transport.

It is believed that the staggered OFETs show stronger gate-voltage dependence than the coplanar devices.[39-41] Basing on the current crowding theory discussed by Richard *et al.*,[39] in staggered OFETs the effective charge injection area is a balance between the channel resistance (R_{ch}) and the contact resistivity (Ω/cm^2). At a small gate voltage R_{ch} is larger than R_C, only a narrow edges of S/D contacts contribute to the charge injection, however at higher gate voltages R_{ch} becomes smaller than R_C, more geometric area will be used for injection to maintain their equilibrium, cf. Fig. 2.16. This is similar to the results observed by Tessler *et al.*,[34] the potential drop peak appears at the source contact edge for small injection barrier, and such a peak moves

to the middle of the source contact when the injection barrier is larger. In fact, this feature is observed not only in OFETs but also in the lightly-doped source-drain (LDD) silicon MOSFETs.[42] The larger injection area leads to more effective contact transport, leading to smaller contact resistance.

On the other hand, the carrier transport in the organic bulk is also significantly modulated by the gate voltage because the charge distribution in the film is not ideally superficial but rather extends to deep bulk. Hence the charge concentration decreases from the OSC/dielectric interface to the contact surface, and such a profile is significantly modulated by the gate voltage, cf. Fig. 2.17. Higher gate voltage gives higher charge concentration and thus higher contact conductivity, leading to a smaller contact resistance. One should also note the above discussed metal penetration, and it will be very an important influence in the TG/BC OFETs and also contribute to the gate-voltage dependent contact resistance.

■ I_{on}/I_{off}

I_{on}/I_{off} is the ratio of the drain current between "ON" and "OFF" state of an OFET and represents the OFETs' capacity for current modulation. In the literature, this ratio is generally reported as the maximum value. In order to increase this ratio, one should increase the maximum current I_{on} and decrease the minimum current I_{off}. For the former, increasing the carrier mobility is a key factor and for the latter, proper synthesis and purification techniques are important to reduce the intrinsic conductivity of OSCs. Note that doping is not a feasible way because it increases the mobility but more rapidly enhances the intrinsic conductivity and thus,[43] the I_{on}/I_{off} falls down with doping concentration, even down to 1.[44, 45]

Because the maximum I_{on} and the minimum I_{off} strongly depend on the applied drain voltage, the maximum I_{on}/I_{off} is usually measured in saturation regime. Meanwhile, it also relies on the channel dimensions, i.e. W and L, hence they should be disclosed for comparison. For real applications, $I_{on}/I_{off} > 10^6$ is often required.

■ Sub-threshold slope

As the applied gate voltage is below the so-called threshold voltage, OFETs work in a sub-threshold region and the sub-threshold slope is defined as:

$$SS = \frac{dV_G}{d(\log I_D)} = \frac{kT}{q} \ln 10 \left(\frac{C_i + C_D + C_{SS}}{C_i} \right) \tag{2.11}$$

where (kT/q) is the thermal voltage, C_D and C_{SS} are the depletion capacitance and the surface states capacitance, respectively. This SS is generally measured at the maximum slope of $\log(I_D)$ versus V_G, and it describes how the switch turns on and off in the subthreshold region. In silicon MOSFETs and at room temperature, $(kT/q)\ln 10 = 60\text{mV}$ and hence the minimum SS is 60mV/decade if C_D and C_{SS} are zero. However, due to the influence of interface states and the substrate bias this parameter is actually greater than 60mV/decade, for example $SS < 100\text{mV}$/decade for conventional Si MOSFETs. Small SS is crucially needed for high switching speed, low-voltage and low-power consumption applications.

Compared to silicon MOSFETs, there are some discrepancies in OFETs. First, the depletion capacitance C_D is zero since OFETs operate in accumulation mode and the depletion layer is not formed,[32, 46] or the intrinsic OSCs film is fully "depleted" as a gate voltage is applied (cf. the relevant modeling in the forth chapter). However, some works assert that in accumulation mode, the thickness of depletion layer becomes nearly zero and hence $C_D \to \infty$.[27] Like this, this value is meaningless and another definition is proposed in this work. For our analysis, C_D is assumed to be zero. Next, the ideal $SS = 60\text{mV}$/decade is the slope of the edge of a Fermi distribution while convolving with an abrupt density of states, e.g., in single-crystal silicon. However, the DOS of OSCs exhibits a gradual rise at the band edge and not all carriers are equally mobile, the

convolution produces a shallower rise in the carrier density and the observed *SS* is much worse than 60mV/decade, e.g. 2V/decade for our pentacene OFETs and around 5V/decade for our PTAA (LITEN, 727) and TIPS pentacene OFETs.

Moreover, hysteresis and charge trapping increase the extraction difficulty since the *SS* is different at the reverse/forward sweeping direction and the significant charge trapping in sub-threshold region causes a non-uniform slope.[27] At the same time, the *SS* strongly depends on C_i, hence many works proposed to normalize *SS* as $SS \times C_i$ for comparison.[47] In any case, the most important use of this parameter is to evaluate the interface states density by $N_{SS}=C_{SS}/q$.[48] The surface states are very important for the single-crystal inorganic transistors due to the presence of dangling bonds at the surfaces.

■ Hysteresis

Hysteresis shifts the threshold voltage between the different sweeping directions of the gate voltage. Strictly, hysteresis is not a parameter of organic transistors but at present it is a critical issue on OFETs' I-V and C-V characteristics. As stated in the classical textbook of S.M. Sze (p402),[25] due to the difference in the permittivity of silicon and gate dielectric(e.g. SiO_2), i.e. $\varepsilon_{Si}/\varepsilon_{SiO2}=11.7/3.9\approx3$, the electrical field could attain a very high level of $(\varepsilon_{Si}/\varepsilon_{SiO2})\times(3\times10^5 V/cm)\approx10^6 V/cm$ in the gate dielectric SiO_2, where 3×10^5V/cm is the field for silicon at avalanche breakdown. Such a strong electrical field cannot cause the electron and hole conduction in the SiO_2 but could provoke a mobile ions transport through the oxide and give rise to device instability and a hysteresis effect. The origin of hysteresis in OFETs is still not well understood up to now and there have been a lot of explanations:[49-52] 1) Trapping and migration of dopant, which was observed in MIS capacitor based on poly(3-hexylthiophene) by Brown *et al.*[53], 2) Slow relaxation of the gate dielectric, especially with polymer-based gate dielectric. The hysteresis in the OFETs with inorganic dielectric is typically less than 1V but it could be as large as 15V in the devices with polymer dielectric.[54] It might be due to the mobile dipole in the bulk of polymer dielectric since the hysteresis effect decreases in thinner polymer film of gate dielectric. These mobile dipoles could originate from: i) molecules or fragments related to external effects, e.g. remaining solvents, impurities or additives in the polymer formulation; ii) macroscopic behavior of the basic polymer; iii) intramolecular dipoles.[55] 3) Dielectric charge storage caused by injection of charge into the gate dielectric. For instance, the gate voltage sweeps from positive to negative, holes are injected into and stored in gate dielectric, thus shifting the threshold voltage to be more negative and screening the gate field. The transfer curve of back sweeping is, of course, shifted to be at more negative gate voltages. 4) Traps in organic semiconductors, which are often related to the moisture, impurities and defects.

Hysteresis strongly depends on the sweeping direction and sweeping rate. In the IEEE 1620 standard, it is recommended that one should keep $V_G=V_D=0$V for 10 minutes after one time of measurement and before move to a next round in order to avoid hysteresis effects.

2.3 FABRICATION METHODS

Due to the different structure and different materials used in organic transistors as compared to Si MOSFETs, their fabrication methods are also different. As the OFETs fabrication involves a wide variety of topics and it is beyond the scope of this thesis, here we focus only on the critical step: deposition of organic semiconductor. Certainly, these techniques could also be applied into other processes, e.g. source/drain and gate patterning.

■ Solution-based deposition

This technique can be used for polymer and small molecule OSCs, including spin-coating, dip coating and printing. This is a very efficient method to realize the organic film of high quality, large surface and low cost, especially the roll-to-roll printing, a promising way for the future organic electronics. The main drawback of this technology is that the semiconductor should be dissolved in solvent. This problem can be overcome by grafting solubilizing groups to the polymer backbone, or by the use of a soluble precursor polymer, which is then converted to the conducting polymers by an appropriate physical and chemical treatment.[45] Another issue of this kind of technique is the low resolution, which typically is around 50-100 μm for the standard offset, gravure, screen or inkjet printing. This technological size possibly provides satisfied switching speed and integration density for the applications such as display but clearly cannot meet the requirements for higher speed mandatory applications, such as RFID tags, because the switching speeds is only in the range of 1-10Hz with typical mobility in solution-processed OFETs.(cf. P296 in Ref.[1]) With the application of self-aligned inkjet printing, the minimum feature size could be as small as 100nm.[56] In the process of reducing this technological size, one more problem arises. This is because the commonly applied flexible substrate, e.g. poly(ethylene terephthalate) PET and poly(ethylene naphthalate) PEN, is very sensitive to the environmental temperature and humidity variation, leading to a large distortion from step-to-step. Such a distortion will cause a number of unforeseen difficulties, such as the misalignment of the gate electrode with the channel pre-defined by S/D. As the solution-based printing meets the roadmap for the future flexible organic electronics with massive production and very low cost, we shall discuss some of main stream printing technologies.

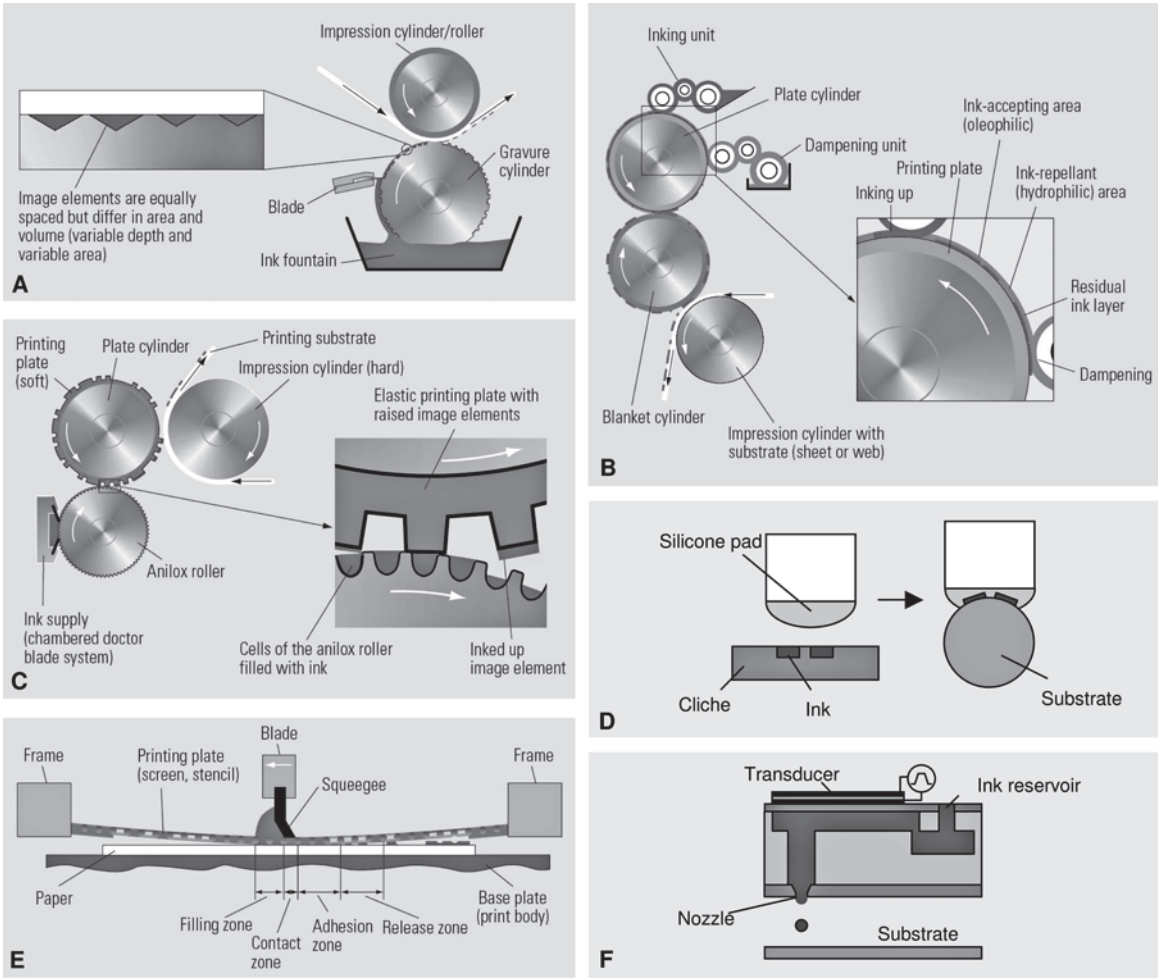

Figure 2.18 | Schematic diagram of operating principles of printing techniques: (A) gravure, (B) offset, (C) flexography, (D) pad printing, (E) screen printing, (F) inkjet printing. (after Sirringhaus 2006 in the book "*Organic Electronics*",[1] P.298)

Screen printing

By this technique, ink is pushed through a screen comprising a fine mesh of plastic or metal fibers, cf. Fig. 2.18E. Patterns are defined by filling the openings of mesh with a stencil. The screen is coated with the ink, and by using a so-called squeegee the mesh is brought into contact with the substrate, the ink is pressed through the openings of the screen to define the desired pattern on the substrate. Screen printing needs the ink having high viscosity, however could be used for a large variety of materials. If an ink of low viscosity is used the precise control of ink flow become difficult, thus degrading the pattern resolution which is determined by the mesh size. At present, the typical resolution of screen printing is at the level of 100μm. Since the produced film thickness is determined by the screen thickness, which could be relative thicker with maintaining reliable printing quality, the resulted film could be rather thick, e.g. >1μm. Up to now, screen printing has been limited in the patterning of top-level interconnects and electrodes, because the related thickness profile doesn't affect the deposition of other critical layers. It is also used to deposit thick and rough layers, such as dielectric and encapsulation layer. The first demonstration of printing OFETs was made by the screen printed graphite source/drain (L=200μm, thickness 10μm) and gate electrodes, and the vacuum evaporated sexithiophene organic semiconductor film.[57] Afterwards, screen printing was also applied to define source/drain (L=100μm, thickness 10μm) electrodes in bottom-gate OFETs with both top-contact and bottom-contact configurations,[58, 59] and to pattern the gate electrode and interconnects in top-gate OFETs.[2]

Offset printing

Offset printing currently is the most widely used commercial printing technique, because of its very high throughout and hence it is very attractive for electronic manufacturing. By this technique, the ink is brought into contact with a printing plate incorporating oleophilic/ink-accepting, and hydrophilic/ink-repellent surface areas. The ink is selectively transferred on to the oleophilic regions of the printing plate, and from there onto the substrate via an intermediate blanket cylinder, cf. Fig. 2.18B. Offset printing has been used to print source/drain electrodes of PEDOT/PSS in top-gate OFETs with L=30-200μm, line width 100-200μm.[1]

Gravure printing

Gravure printing is also a very high-throughout technique, but it is often limited in the print runs more than a million copies due to the high cost for making the engraved cylinder. It is based on a metal cylinder with an engraved or etched pattern of cells, which are filled with ink by doctor blading, cf. Fig. 2.18A. The cells can be of diverse size and depth, and are used to transfer the ink onto a flexible substrate when the latter is brought into contact with the rotating cylinder. Gravure printing could print low viscosity ink form volatile solvents and hence, be easier to produce low film thickness without using additives as compared to offset printing. Because in offset printing, the ink formulation is a big challenge to simultaneously meet the requirements of ink viscosity, surface tension, evaporation rate, high-quality structures on a given substrates and optimum device performances, additives are sometimes needed. Till now, gravure printing has not yet been used for OFETs fabrication.

However, an associated non-continuous and lower-throughout technique is pad printing which has been used to pattern etch resist onto a film of polyaniline in order to define source/drain electrodes with L=20-60μm, line width >100μm in top-gate OFETs. A flexible silicone stamp is applied to pick up ink from a cliché to transfer it onto a substrate which can have a nonplanar shape, cf. Fig. 2.18D. A conducting carbon-based ink was also pad-printed to define bumps for via-hole interconnections and gate electrodes.

Flexography

The principle of flexography is similar to that of common letterpress technique but the printing plate is flexible in flexography. This technique is widely used for packaging where the lower printing quality with respect to offset and gravure printing can be tolerated. A pattern of protruding and ink-receptive regions are separated by nonprinting wells, which is inked by using an anilox roller, cf. Fig. 2.18C. The ink can be transferred from the protruding regions of the plate onto a broad range of absorbent and nonabsorbent substrates. This technique, to date, has not been applied for OFETs fabrication.

However, a related laboratory technique, soft lithography, has been applied to make some components in OFETs. For instance, polydimethoxysilane (PDMS) stamp is inked with a self-assembled monolayer (SAM) which can be selectively transferred to the substrate from the protruding regions of the stamps. The SAM patterns made by this way have been used as etch masks for etching gold source/drain electrodes with high resolution.[60, 61] The channel length could be as short as 0.1μm by employing PDMS stamps as phase shift masks in the photolithography procedure of gold source/drain electrodes.[62] Soft lithography has also been proposed to be used in reel-to-reel printing.[60] Generally, both flexography and soft lithography suffer from stamp distortions, degrading accurate pattern registration over large area.

Inkjet printing

Inkjet printing is a promising technique for organic electronics manufacturing in spite of its relatively lower throughout with respect to gravure printing. It could provide high resolution and mostly ease of formulating inkjet printable inks for a broad range of functional materials. Inkjet printing (7th generation) has been applied to LCD fabrication for printing of color filters and other components or polymer light-emitting diode (LED) displays for patterning the red, green and blue-emitting polymers. The most common inkjet technology for printing electronics materials is drop-on demand (DOD) printing, cf. Fig. 2.18F. In thermal DOD printing, droplets are generated by heating the wall of ink chamber, forming vapor bubbles and ejection of droplets through a nozzle orifice. In piezoelectric DOD printing, a pressure wave in the ink chamber is generated by applying a voltage pulse to a piezoelectric stack or plate, resulting in formation of droplets at the nozzles. Piezoelectric DOD inkjet printing has been used to direct-write patterning of PEDOT/PSS conducting polymer as source/drain electrodes[63] and of nanoparticle metal electrode as well as interconnections.[64] The state-of-the-art linewidths is at the level of 20-100μm with droplet volumes of 1-30 pico-litre(pL). Active semiconducting layers could also be inkjet patterned either by direct printing of polymer semiconductor inks[65] or by patterning of mask patterns for SAM surface energy patterns to induce selective dewetting of the active semiconducting materials.[66] A process for definition of via-hole interconnections by inkjet printing of solvent for local etching/dissolution of continuous dielectric and semiconducting layers has also been reported.[67]

Vacuum evaporation

This method is generally used for small molecule OSCs which are difficult to be dissolved in the solvents, e.g. pentacene. These materials are often used in OFETs in the form of thin film which could be grown by different processes: physical vapor deposition (PVD), chemical vapor deposition (CVD), pulsed laser deposition (PLD) and ion sputtering, depending on the chemical nature of the source OSC materials and the desired film properties. Vacuum deposition occurs as molecules are removed from a solid or liquid and subsequently travel over a distance in a vacuum chamber and impinge on the substrate at a rate, which is usually measured in monolayer per second. Typical vacuum chamber used for PVD is shown in Fig. 2.19a and it is equipped with a bell jar, vacuum pump, boat (on which the OSC materials are heated to the sublimation or evaporation temperature), shutter, substrate mount and quart crystal microbalance that is used to measure the film thickness. A custom-made chamber at the Cornell high-energy synchrotron source is

shown in Fig. 2.19b, in which a beryllium window is installed to allow the transmission of x-rays onto the substrate. Compared to the deposition of inorganic materials, the film growth of organic film is much more complex. For instance, the binding energies in molecular crystal are highly anisotropic due to the complex shape of molecules, causing the inherent anisotropy in the crystal packing. The lack of true epitaxy with the substrate because of the usually inert and amorphous substrates leads to a molecular arrangement with a preferential orientation along one crystallographic direction, e.g. pentacene's [001] parallel to the normal of the surface. Another issue on complexity relative to inorganic materials deposition is the much weaker intermolecular binding energies in OSC materials, reducing significantly the range of deposition temperature.

The performances of OFETs fabricated by this technique are found to strongly depend on the film morphology. With well controlling the deposition temperature and surface roughness of the substrate as well as the deposition rate, one can obtain a very thin with very precise thickness and very highly ordered film. Because the deposition is finished in vacuum, the resulting purity of OSCs can be up to crystalline level and therefore, it often affords the highest mobility. Note that polymers cannot be made by this technique, since they cannot withstand high temperature and will be decomposed at high temperature. The inconvenience is that it requires sophisticated instrumentation, long pump-down time, and thus technologically punishes the fabrication cost.

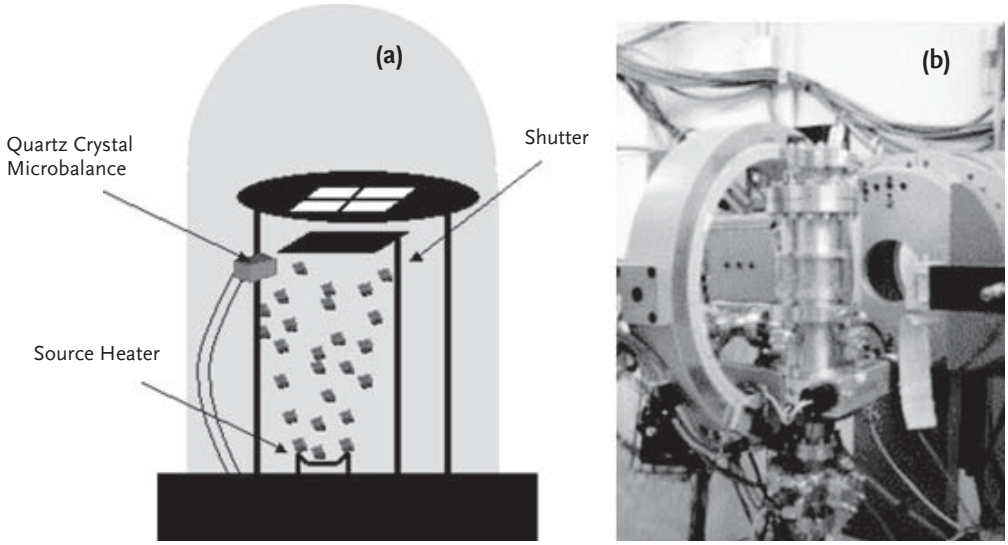

Figure 2.19 | (a) PVD vacuum systems used for thin film deposition. (b) Chamber mounted at the A2 station at the Cornell high-energy synchrotron source. (after Mayer *et al*. 2007 in the book "*Organic Field-Effect Transistorss*",[1, 7] P.342)

■ Organic vapor phase deposition (OVPD)

The previously discussed vacuum deposition is similar to the conventional molecular beam epitaxy (MBE) and has limitations in process control, flexibility, scalability and cost effective manufacturing capability. So, metal organic vapor phase deposition (MOVPD) replaces MBE for production of III-V semiconductors. At present, the inorganic ultra high brightness LED can be only made by MOVPD in industrial production. In 1995, S. Forrest introduced the organic vapor phase deposition (OVPD) at Princeton University to take advantage of the benefits of gas phase process in organic electronics. Because the arrangement of evaporation and condensation is decoupled in OVPD, the limitations of vacuum thermal evaporation could be overcome and thus the evaporation could be optimized for any chemical requirements without affecting the uniform deposition of large-area organic film.

As seen in Fig. 2.20, two kinds of source organic materials in decoupled quartz pipe are separately evaporated and very precisely picked up to quartz chamber by standard mass-flow

controlled (MFC) carrier gas, e.g. N_2. The two sources materials in gas phase are uniformly mixed in the hot wall deposition chamber, they diffuse through the boundary layer and condense onto the cooled substrate. This deposition of expensive organic materials is mainly taken place on the substrate not in the chamber, improving the efficiency in the use of materials. Due to the use of carrier gas, the pressure of OVPD is around of 10^{-3}-10 torr, thus it is not necessary to consume much time to pump down the large chamber for high vacuum condition. Meanwhile, the continuous purge of carrier gas could prevent the contaminations, thus increasing the reproducibility of the deposited organic film quality. So OVPD is expected to be an ideal solution for industrial mass production and has already been applied to fabricate OLED for displays and lighting, organic photovoltaic cells and OFETs.

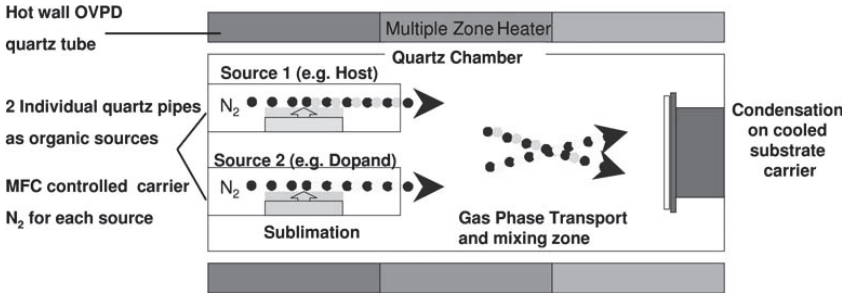

Figure 2.20 | OVPD principle and quartz flow deposition module invented by Forrest. (after Heuken *et al*. 2006 in the book "*Organic Electronics*",[1] P.203)

Table 2.1 summarizes the main properties of OVPD with comparison of the conventional vacuum thermal evaporation (VTE). 1, As discussed above, VTE necessitates high vacuum conditions which expends much more time to pump down with respect to OVPD where the use of carrier gas enables a relative higher pressure. 2, The close coupled showerhead OVPD could provide homogeneously distributed organic materials in gas phase and with two-dimensional scalability, thus very suitable for the deposition on large-area substrate. However, in conventional VTE the organic materials are put as a point source, thus leading to a three-dimensional scalability. Introduction of linear source to VTE improves the scaling but needs to increase the evaporation temperature to remain the same deposition rate. 3, In OVPD, due to the intermolecular collisions coming from the carrier gas molecules, the source organic molecules are randomly distributed in the deposition chamber and thus, giving rises to a uniform film. This feature could even compensate the substrate non-uniformity originating from defects and particles. So OVPD could be applied into complex three-dimensional structured substrates. Whereas in VTE, the molecule transport can be described as a ballistic process, the geometry of the source (i.e., point, multi-point and linear sources) will be directly reflected by the film thickness uniformity and the layer coverage on the substrate, sometimes even leading to pin-holes. For this, rotating the substrate and randomizing the ballistic trajectories are often applied to improve those problems. 4, Precise control of the amount of source organic materials could enable very high film thickness reproducibility in OVPD and similarly enable precise coevaporation or doping of σ<0.5% by controlling the multiple sources, e.g. host and dopant. However in VTE, the precise coevaporation of doping can be achieved by adjusting the crucible temperate but it will exponentially change the deposition rate, thus the doping is difficult to be precisely controlled. 5, The transport of all organic materials into the deposition chamber in OVPD could prevent any cross contamination. 6, The precise adjustment of the amount of source organic materials by MFC in OVPD is difficult being applied in VTE, where the similar control is realized by controlling the evaporation temperature. However it will affect the resulted film roughness and morphology. 7, In OVPD, all the source organic materials are transported into the deposition chamber by carrier gas, the material utilization could be as high as 50-70%, contrasting to that in VTE

where it can attain to only 1-6%. This is because of huge parasite surface which consumes the vast majority of the expensive organic materials. 8, Such a high material utilization efficiency with hall wall design and the continuous purge of carrier gas in OVPD also reduce the particle formation and thus, lowering the maintenance cost and the downtime. 9, As discussed, the deposition rate could be very precisely controlled by MFC adjusting the amount of carrier gas, the reproducible high deposition rate is 30Å/s. However in VTE, the same control of deposition rate realized by adjusting evaporation temperature can give 1-10Å/s, at the same time it significantly affects the film quality and thus the performances of final devices. Therefore, the high evaporation rate of OVPD is very suitable for industrial mass production. 10, Another advantage of OVPD over VTE is to control the surface morphology. For instance, by using two different deposition modes, one can design the layer morphology and interfaces, which is very useful to improve the devices performances.

TABLE 2.1. Intrinsic process characteristics of close coupled showerhead OVPD technology compared with conventional vacuum thermal evaporation (VTE)

No.	Process properties	OVPD	VTE
1	Pressure	10^{-3}-10 Torr	$<10^{-6}$ Torr
2	Scalability	Two-dimensional	Three-dimensional
3	Layer uniformity	(~1%)	(~3%)
4	Doping control	<0.5%	>2%
5	Cross contamination	Low	High
6	Thickness control	~5-10Å	~5-10Å
7	Deposition efficiency (material utilization)	50-70%	<15%
8	System downtime	Low because of hot wall design	High because of particle generation
9	Deposition rate	~30Å/s	~3-10Å/s
10	Morphology control	Tunable	Difficult to control

(after Heuken *et al*. 2006 in the book "*Organic Electronics*",[1] P.226)

■ Electropolymerization

This is a leading technique for the synthesis of conducting polymers and the first OFET was fabricated with polythiophene by this technology. It begins from a solution of monomer which is subsequently polymerized after electrochemical oxidation. The polymer is firstly grown on the conductive surface (e.g. source and drain electrodes) and next extends to other non-conductive surfaces. In consequence, the arrangement of organic semiconductors is not good, especially around the contacts; the interface quality of OSC/dielectric is not good. In addition, the obtained polymers are in its oxidized state and it should be reduced to become semiconductor, more disorders are thus induced. Therefore, this technique is no longer used in the OFETs' fabrication.[45]

■ Langmuir-Blodgett technique

The organic film (generally in small molecule) obtained by this technique possess very thin thickness and very highly order. However, this method is restricted to amphiphilic molecules, composed of a hydrophobic chain and a hydrophobic head-group, which is not the case for most molecules used in OFETs.

2.4 SAMPLES USED IN THIS THESIS

In this thesis, we study several groups of OFETs provided by three institutions: IZM (Germany), RIKEN&NIMS (Japan) and CEA-Liten (Grenoble, France)

■ Pentacene OFETs (RIKEN&NIMS)

We firstly studied two sets of TC and BC pentacene channel OFETs, as shown schematically in Fig. 2.21(a). They were fabricated on heavily doped Si (100) wafers covered with a 50nm thick SiO_2 layer, which ultimately serve as the gate electrode and the gate insulator, respectively. After cleaning the surface with organic solvents and acids, a self-assembled monolayer (SAM) of octadecyltrichlorosilane (OTS) was formed on the SiO_2 surface. That procedure is known to reduce the concentration of interface states. The fabrication of the BC and TC OFETs differs in the sequence of organic semiconductors layer and metal electrodes deposition. For the former, the source and drain electrodes are deposited directly on the SiO_2 surface. Here that was done by a sequential evaporation of 5-nm-thick MoO_3 and 35-nm-thick gold through a metal mask. Next a pentacene (Aldrich, purified using temperature gradient sublimation) layer was vacuum-deposited (rate of 0.01 nm/s at room temperature, final thickness of 50nm). In the TC devices the pentacene layer was deposited first and then the source and drain electrodes were formed by thermal evaporation of Cu through a metal mask. Fig. 2.7b shows a laser beam microphotograph of the near-contact region in a BC device with a small grain zone, which probably affects device performance. The chemical structure of pentacene molecule is shown in Fig. 2.21b.

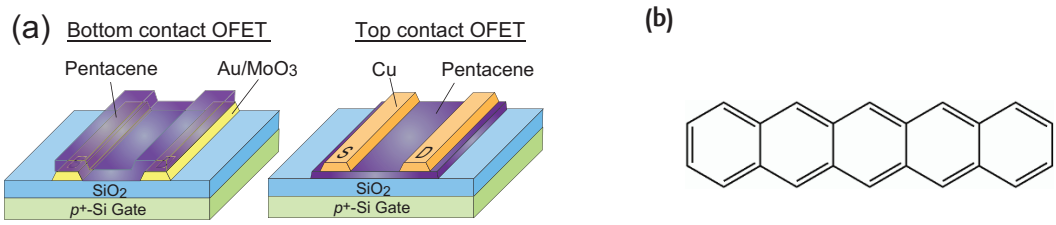

Figure 2.21 | (a) Schematic illustration of TC and BC pentacene OFETs. (b) Chemical structure of a pentacene molecule.

Afterwards, we studied three sets of TC pentacene OFETs and the pentacene film thickness is controlled to at 20nm, 50nm and 100nm, respectively. However, the set of transistors of the thinnest film cannot operate correctly and hence, one studied only the other two sets.

■ PTAA OFETs (IZM)

Fig. 2.22a shows a schematic cross-section to illustrate the layer sequence of the fabricated devices. As basis a PET foil metalized with 0.5µm thick copper is used. To improve adhesion to the polymer film an additional tie layer of chromium is used. This metallization is patterned by means of photolithography, which needs several process steps. First dry resist is laminated and then UV exposure is done on a CIPOSA 2200 system for reel-to reel exposure and mask alignment. Afterwards the resist is developed in alkaline soda solution. Copper and chromium are etched in $Na_2S_2O_8$ resp. $K_3Fe(CN)_6$ solution and finally the resist is stripped in 3% KOH solution. It should be pointed out, that these steps have been performed on a roll of foil with a width of 210 mm at a speed in the range of 0.5 to 1 m/min. The photolithographic patterning process allows high resolution with minimum feature sizes of 10 to 15µm. 20µm pat-

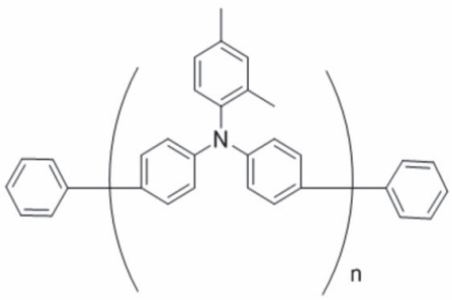

Figure 2.22 | Chemical structure of a monomer of PTAA.

terns are fabricated with high reproducibility and nearly 100% yield. Scaling towards even lower dimensions will be possible, but currently this is limited by the thickness of the used dry resist (18μm).

The further layers are built up by two coating and three screen printing steps. Polytriarylamine (PTAA) is used as semiconductive layer, because of its excellent stability under ambient atmosphere. As gate dielectric a low-κ material has been used, because of the better interface between organic semiconductor and dielectric layer. Both materials have been supplied in suitable solvent formulations by Avecia Ltd. For coating a blading method capable of performing continuous coating has been used. It turned out that the coated films still do not show sufficient quality and uniformity, so that in consequence this process still has to be further developed. For evaluation of the principle fabrication method, spin coating has been used additionally, although the general reel-to-reel approach is left by this. This causes that the roll with patterned copper has to be cut into single sheets with dimension of 200×200mm². Spin coating on this quite large sheets deliver semiconductor and gate dielectric layers with the necessary quality. Each layer has been dried in an oven at 100°C for 10 minutes.

Screen printing is done with a reel-to-reel screen printer (Aurel VS1520M) which is capable of printing on rolls as well as on sheets. Different screens are used to print gate electrodes, multilayer dielectric and the final wiring with silver-filled paste. Especially screen printing of the gate turned out to be a very critical step since it has to be avoided to damage the underlying thin insulating dielectric layer. Two possible failure mechanisms are observed. Solvent of the printed paste can dissolve the dielectric layer before curing or filled particles can mechanically damage this layer. Both mechanisms lead to excessive leakage currents between gate electrode and the semiconducting channel. We therefore decided to use a water-based formulation of PEDOT/PSS for gate electrodes instead of filled or solvent based pastes. Screen printing of multilayer dielectric defines the vias to gate and source-drain conductors. Before printing the final top wiring the dielectric and semiconductor material must be removed in the vias. This is done with solvent and is a quite critical process. At the beginning we used toluene as solvent with the result that gate material and multilayer dielectric peeled off partly. The reason for this was strong under creep of the solvent between foil and multilayer dielectric. Thus we are using less strong solvents for via opening. This has the disadvantage that the dielectric isolation layer can be removed quite well, but there is the risk that semiconductor residuals remain at the bottom of the vias. The whole fabrication process including the bladed films has been performed on a roll of PET. The result is shown Fig. 2.22b. Due to the problems with the quality of the bladed films the electrical characterization results for the hybrid manufacturing process is based on sheets with spin-coated layers of polymer semiconductor and dielectric. Nevertheless it can be expected that these results will be also transferable to a full reel-to-reel process.[2]

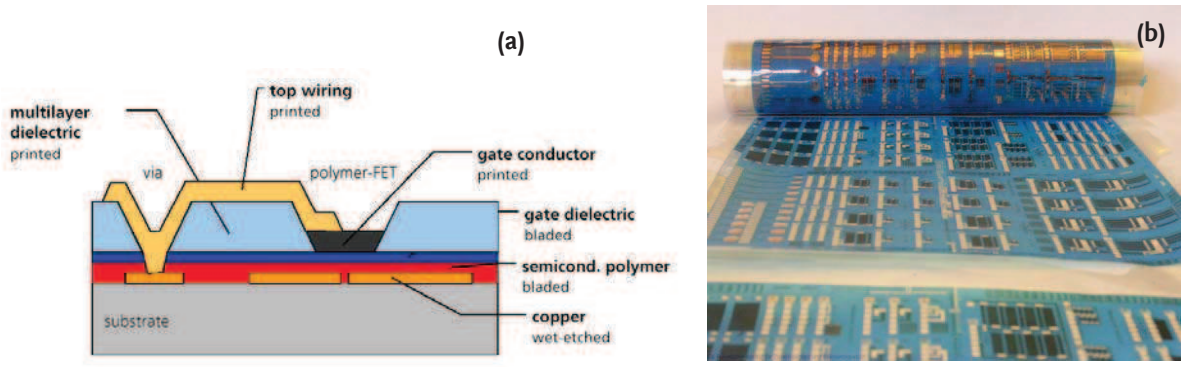

Figure 2.23 | (a) Schematic illustration of reel-to-reel printing OFETs (b) Reel-to-reel processed foil with polymer test patterns (After Klink 2005[2])

■ PTAA OFETs and n-type OFETs (CEA-Liten)

Four sets of PTAA OFETs made by CEA-Liten were studied in this thesis. The first three sets have the same layout, as shown in Fig. 2.23, and their substrate codes are 379, 383 and 404. Next, a new generation of PTAA OFETs having much higher performances and with layout view seen in Fig. 2.24 was analyzed, and the corresponding substrate code is 727. Meanwhile, a set of n-type OFETs were examined, the layout of the substrate (code 729) is the same as that of 727.

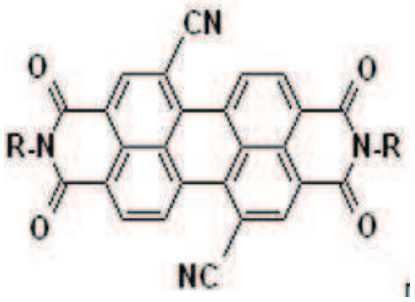

Figure 2.24 | Chemical structure of a molecule of N1400.

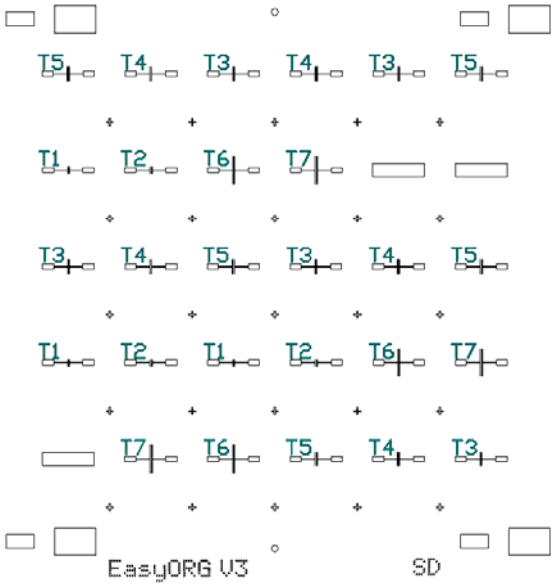

Figure 2.25 | Layout view of the printing PTAA OFETs on substrate 379, 383 and 404.

The organic devices are fabricated on gold-plated 125µm-thick polyethylene-naphtalate (PEN), using a top gate structure for both n and p-type devices. The 30nm gold layer is patterned by photolithography with a line/space resolution down to 5µm, forming the source and drain electrodes as well as the 1st level of interconnection lines between gates. N-type organic semiconductor (perylene diimide derivative) is deposited in solution by direct printing methods, defining patterns corresponding to individual devices and annealed under ambient atmosphere at 100°C, leading to a final thickness in the range of 50-200nm. P-type organic semiconductor (poly-triarylamine derivative) is then deposited by the same method and annealed, with a final thickness also in the 50-200nm range. The gate dielectric polymer is printed on the top of both semiconductors and then annealed, leaving open areas for via holes, with a final thickness of 1µm. Finally, a silver-ink conductor is printed on the top of dielectric and annealed at 100°C, forming in the same step the gate electrodes for devices and the 2nd level for interconnection.

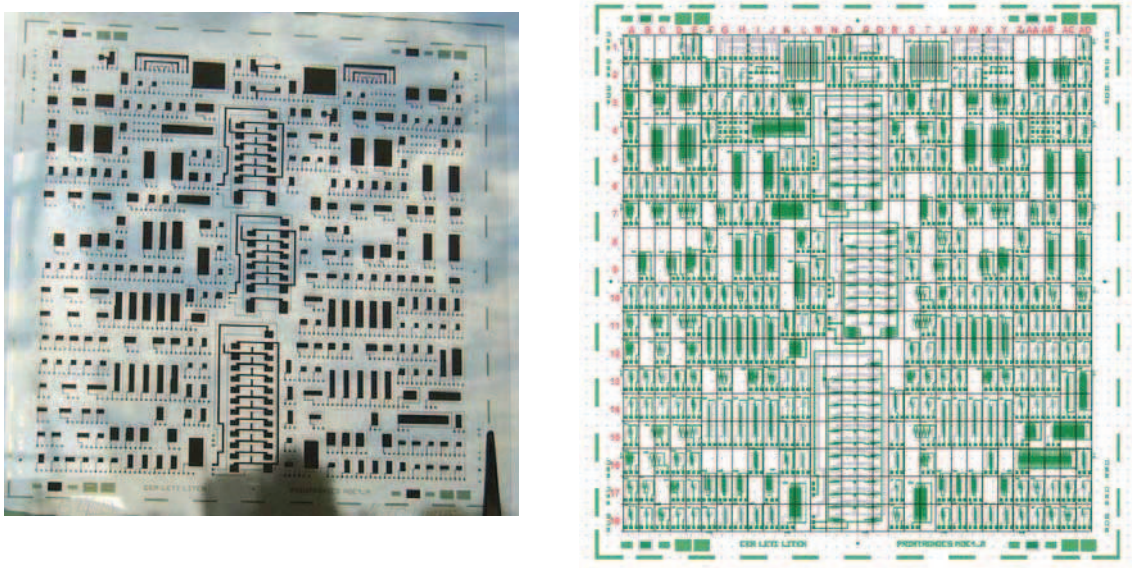

Figure 2.26 | (a) Image of the final substrate for 727(PTAA), 729(N-type) and 715(TIPS-pentacene). (b) Layout view of the same substrate as in (a).

■ TIPS-pentacene OFETs(CEA-Liten)

A final set of TIPS-pentacene OFETs were received from CEA-Liten. These OFETs show remarkable high quality and high performance. The substrate layout is the same as shown in Fig. 2.24 and the substrate code is 715.

A polymer PEN (Teonex Q65FA) film is chosen as substrate since it is an emerging leader material for OLED displays and active matrix backplanes. The substrate is provided with covering a 30nm thick Au layer on the surface which is cleaned by exposure to ultra sound in acetone and isopropanol (IPA) and then pre-treated and heat stabilized with high clarity Tg at 120 °C and Tf at 260 °C. The final PEN film thickness is around 125 μm and a clean and smooth surface is obtained. The Au layer is subsequently ablated by laser, and the left gap defines the channel length. The laser ablation is compatible with the roll-to-roll process and provides high speed, mass production, low cost and high resolution, all of which are required for the future printing technology. After S/D definition and cleaning process, the organic semiconductor (OSC) of polymer-small molecule blend (TIPS-pentacene) is deposited by gravure printing, the average thickness of OSC film is about 100nm. Over the TIPS-pentacene film, a solution of Fluoropolymer Cytop™ with fluorosolvent (orthogonal) is deposited, which is used as the gate dielectric. The thickness is around 800-1200 nm that corresponds to $C_i \approx 2\times10^{-9}\mathrm{Fcm}^{-2}$, confirmed by C-V characteristics. Cytop™ is known as a high performance material for the gate dielectric because of its high breakdown strength, extremely low impurity concentration, good environmental stability and good compatibility with other processes. Finally, the gate (silver paste) level is printed. The small grains are sometimes obtained and this is due to the sensitivity of OFETs' performances to the external contaminations, substrate surface and OSC/dielectric interface quality, thus all the processes including preparing are finished in a clean room or glove box. The final OFETs exhibit high performance and good quality, e.g., the grain size of TIPS-pentacene is large, cf. Ref.[68]

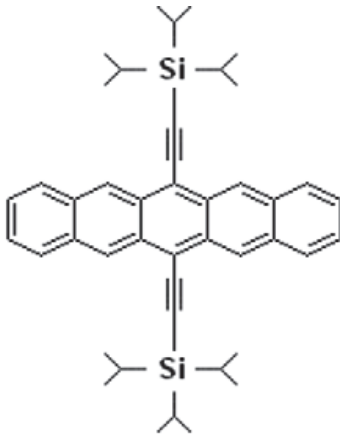

Figure 2.27 | Chemical structure of a molecule of TIPS-pentacene

2.5 CONCLUSIONS

In conclusion, a full view of organic transistors has been presented. One first examined the OFETs' structures (configurations), OFETs apply a thin film of organic materials instead of the single-crystal bulk in silicon MOSFETs and thereby, OFETs are also often referred to as OTFTs. Because of the different location of gate and S/D electrodes, there are four configurations for OFETs fabrication and each configuration has their own advantages and disadvantages. Next, we discussed the OFETs' operating mechanism and they work nearly similarly to the conventional MOSFETs. The only one difference is that the depletion/inversion of Si MOSFETs is absent in OFETs due to the intrinsic organic semiconductors and the thin film structure, the charge is injected from contacts into the organic film thus the OFETs operate directly in accumulation mode while a proper gate voltage is applied. And then, we analyzed the OFETs' principle parameters: mobility, threshold voltage, contact resistance, subthreshold slope etc. The relevant issues and critical results in the literature have also been addressed. Finally, we investigated the principal techniques for organic transistors fabrication. In the next chapter, we will focus on the OFETs electrical characterization which is the prerequisite for the subsequent modeling work.

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Chapter 3
Electrical characterizations

With respect to the well developed methods for the electrical characterizations of silicon MOSFETs, the methods presently used for organic transistors are very limited. This might be due to the different structure and the different operating mode. However, the organic transistors work also as normal field-effect transistors (FETs) and exhibit same output/transfer characteristics as Si MOSFETs. Hence the rich resource of Si MOSFETs can be applied to OFETs' electrical characterizations.

In this chapter, we will first present the commonly used methods for carrier mobility and threshold voltage extraction in current OFETs community. And then, a Y function method (YFM) is introduced to evaluate the low-field mobility, threshold voltage, contact resistance etc. Next, we will separately discuss the principal OFETs parameters extraction and the relevant issues. During discussion, some experimental results are used to illustrate the analysis process.

3.1 CLASSIC METHODS

Two classical methods are commonly employed with a hypothesis of constant carrier mobility. With regard to the parameter evaluation, the transfer characteristics are more used and the output characteristics are often used to observe the OFETs functionality.

■ Linear regime (at small drain voltages)

When a small drain voltage is applied, the OFETs operate in linear regime and the drain current follows:

$$I_D = \frac{W}{L}\mu_{eff} C_i (V_G - V_T) V_D \qquad (3.1)$$

where μ_{eff} is the effective mobility which is generally measured at small drain voltages. From this equation, the transconductance g_m can be obtained as:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{W}{L}\mu_{eff} C_i V_D \qquad (3.2)$$

It is clear that g_m describes the slope of the drain current variation with respect to the gate voltage. So, we could extract two parameters by this plot, as shown in Fig. 3.1.

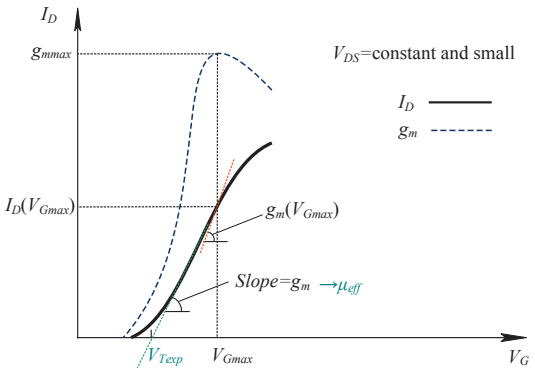


Figure 3.1 | Transfer characteristics in linear regime. The effective mobility and the extrapolated threshold voltage are extracted.

■■ Effective mobility

$$\mu_{eff} = \frac{slope}{(W/L)C_i V_D} \qquad (3.3)$$

■■ Extrapolated threshold voltage

$$V_{Text} = V_{G\max} - \frac{I_D(V_{G\max})}{g_m(V_{G\max})} \qquad (3.4)$$

where $V_{G\max}$ is the gate voltage at which the transconductance attains its maximum value $g_{m\max}$. Note that the extrapolated threshold voltage from transconductance is not exactly equal to the charge threshold voltage, as discussed later.

■ **Saturation regime (at high drain voltages)**

If a high drain voltage is applied, the OFETs will work in saturation regime and in this case, the drain current doesn't depend on the drain voltage any more and obeys the relationship below:

$$I_{Dsat} = \frac{W}{2L}\mu_{sat}C_i(V_G - V_T)^2 \qquad (3.5)$$

Taking the square root of the drain current as:

$$\sqrt{I_{Dsat}} = \sqrt{\frac{W}{2L}\mu_{sat}C_i}(V_G - V_T) \qquad (3.6)$$

A saturation field-effect mobility μ_{fe} is often obtained from its plot as a function of the gate voltage, as shown in Fig. 3.2. The intercept of the linear fitting line in V_G axis gives the threshold voltage. Thus,

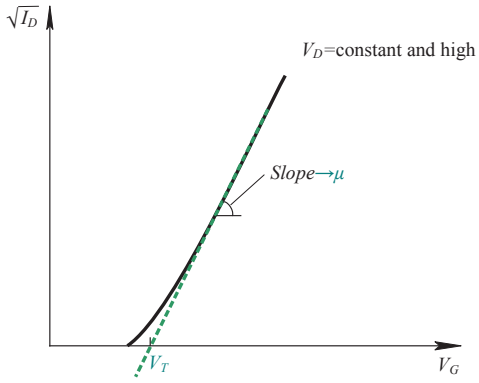


Figure 3.2 | Transfer characteristics in saturation regime. The saturation field-effect mobility and the threshold voltage can be extracted.

■■ **Field-effect mobility in saturation regime**

$$\mu_{sat} = \frac{slope}{\sqrt{(W/2L)C_i}} \qquad (3.7)$$

■■ **Threshold voltage:** V_T, as seen the intercept of the fitting straight line in the V_G axis.

The second method (in saturation regime) is the most widely used method for the carrier mobility and threshold voltage evaluation in the OFETs community now. This is because in linear regime, the drain current is often limited by the contact resistance and/or other additional effects, causing an underestimation of mobility.[1] But one should also note the saturation effects, e.g., the gate/drain voltage dependent mobility and the short-channel effect. For the former, the non-uniform channel (non-uniform local potential drop along the channel) leads to non constant average mobility along the channel.[2, 3] For the latter, if the channel length is comparable to or only few times greater than the organic film thickness, the drain current doesn't saturate at the expected value $V_{Dsat}=(V_G-V_T)$, in particular at low temperatures.[4] Like this, the mobility and the threshold cannot be extracted.

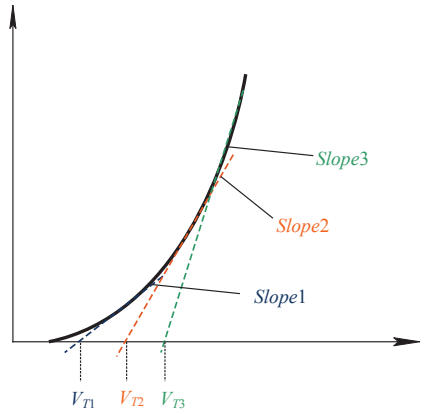


Figure 3.3 | Illustration of the influence of arbitrarily selected data for mobility and threshold voltage evaluations, which require a good linearity in both the classical methods.

The two classic methods are easy to use but not very reliable because a good linearity sometimes cannot be attained,[5] as seen in Fig. 3.3. Hence the mobility and the threshold voltage are not accurately evaluated. In addition, a critical parameter in OFETs, contact resistance, is not available by those methods. Therefore, a more reliable and more powerful parameter extraction method is needed.

3.2 Y FUNCTION METHOD

The Y function method (YFM) was established for the parameters extraction of silicon MOSFETs,[6] based on the dedicated expression of transfer characteristics $I_D(V_G)$. It has been

proved to be a simple but powerful method to extract low-field mobility, threshold voltage, contact resistance, mobility attenuation factor etc. Its important feature for organic transistors is not only to evaluate the low-field mobility without the contact resistance influence, but also to extract the contact resistance from individual transistors, which meets simultaneously the two critical and urgent requirements in the OFETs field.

In linear regime, the transfer characteristics I_D-V_G can be expressed as:

$$I_D = g_D \times V_D = \frac{W}{L} Q_i \mu_{eff} \times V_D \tag{3.8}$$

where g_D is the channel conductance, V_D is the drain voltage, Q_i is the channel charge per unit area, and μ_{eff} is the effective mobility. Moreover, the μ_{eff} is a first order function of Q_i as:

$$\mu_{eff} = \frac{\mu_0}{1 + Q_i / Q_c} \tag{3.9}$$

where μ_0 is the low-field mobility(at small V_D), which characterizes the intrinsic carrier mobility and is the upper limit of carrier mobility expected for a given material/transistor under ideal conditions. Q_c is the critical charge, which represents the mobility attenuation at high gate field, the typical value for silicon MOSFETs is around 10^{13} q/cm^2.

We have the transconductance g_m by the differential of I_D on V_G:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{W}{L} C_i V_D \frac{C_{acc}}{C_i + C_D + C_{ss} + C_{acc}} \times \frac{\mu_{eff}^2}{\mu_0} \tag{3.10}$$

where C_{acc}, C_D and C_{ss} are the unit area capacitance of the accumulation layer, depletion layer and interface states, respectively. Generally, we assume C_D=0 in OFETs. By normalization, one obtains the field-effect mobility μ_{fe}:

$$\mu_{fe} = \frac{g_m}{(W/L) C_i V_D} = \frac{C_{acc}}{C_i + C_D + C_{ss} + C_{acc}} \times \frac{\mu_{eff}^2}{\mu_0} \tag{3.11}$$

If a small gate voltage is applied, i.e. C_{acc} is very small, C_i will dominate the denominator of the first term of Eq. 3.11(right side) and hence, μ_{fe} varies significantly with V_G. On the other hand, if the applied gate voltage is very high C_{acc} is much greater than C_i and C_{ss}, μ_{fe} stabilizes with V_G and approaches to μ_{fe}^2/μ_0, as seen in Fig. 3.4. It is clear that μ_{eff} decreases with V_G or Q_i in strong accumulation. Next, we separately address the electrical properties in weak and strong accumulation.

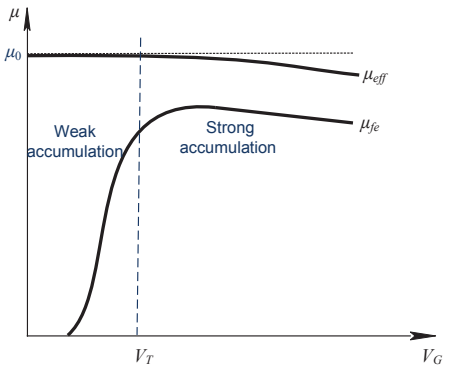


Figure 3.4 | Illustration of three mobilities variation with respect to the gate voltage.

■ Weak accumulation

Applying a small V_G less than V_T, the surface potential on both sides of the OSC film increases linearly with V_G (discuss later)and thus, the drain current I_D varies exponentially with V_G.[7]

$$I_D = \frac{W}{L} \mu_0 C_i \frac{kT}{q} \exp\left[\frac{q(V_G - V_T)}{kT} \frac{C_i}{C_i + C_D + C_{ss}}\right] \times V_D \tag{3.12}$$

If we take the logarithm of Eq. 3.12, one will have:

$$\ln(I_D) = \frac{q(V_G - V_T)}{kT} \frac{C_i}{C_i + C_D + C_{ss}} + \ln\left(\frac{W}{L} \mu_0 C_i \frac{kT}{q} V_D\right) \tag{3.13}$$

Because the second term is a constant, the differential with respect to V_G gives:

$$\frac{\partial \ln(I_D)}{\partial V_G} = \frac{q}{kT} \frac{C_i}{C_i + C_D + C_{ss}} \tag{3.14}$$

Therefore, a characteristic of subthreshold slope (*SS*) can be defined as:

$$SS = \frac{\partial V_G}{\partial \log(I_D)} = \frac{kT}{q} \ln 10 \frac{C_i + C_D + C_{ss}}{C_i} \tag{3.15}$$

This parameter is often used to extract the interface states density by $N_{ss}=C_{ss}/q$.

■ Strong accumulation

If a high V_G is applied, the surface potentials saturate with V_G, hence the Q_i increases linearly with V_G, giving an charge approximation $Q_i \approx C_i(V_G - V_T)$. Replace Q_i by $C_i(V_G - V_T)$ in Eqs. 3.8, 3.9, one obtains:

$$I_D = \frac{W}{L} C_i (V_G - V_T) \frac{\mu_0}{1 + \frac{C_i (V_G - V_T)}{Q_c}} \times V_D = \frac{W}{L} C_i (V_G - V_T) \frac{\mu_0}{1 + \theta (V_G - V_T)} \times V_D \tag{3.16}$$

where $\theta = C_i/Q_c$, is the mobility attenuation factor. As θ is multiplied with $(V_G - V_T)$ in the denominator, it describes the effective mobility degradation with the gate voltage, as seen in Fig. 3.4. In a real transistor, there are several mobility attenuation effects: phonon scattering, surface roughness scattering and contact resistance etc., among which the contact resistance is a crucial one for organic transistors. Hence we shall analyze its impact and find out its extraction method.

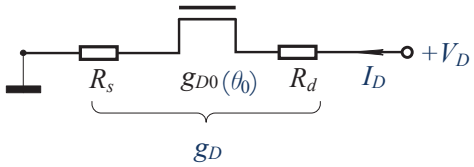


Figure 3.5 | Equivalent schema of a transistor operating in linear regime, here we only consider the contact resistance attenuation on the effective mobility. The pure channel conductance and the overall output conductance are denoted as g_{D0} and g_D, respectively. The individual access on source and drain side are represented by R_s and R_d,

In linear regime, the OFETs can be regarded as a linear resistance controlled by V_G. The total output conductance is denoted as g_D, comprising two contributions: channel resistance and access/contact resistance, as shown in Fig. 3.5. If we combine the source and drain access resistance together, i.e. $R_{sd}=R_s+R_d$, the total output conductance can be written as:

$$g_D = \frac{1}{R_{sd} + \left(1/g_{D0}\right)} = \frac{g_{D0}}{1 + R_{sd} g_{D0}} \tag{3.17}$$

where g_{D0} is the channel conductance alone. Because the contact resistance is the unique mobility attenuation contribution here, thus g_{D0} could be replaced by:

$$g_{D0} = \frac{W}{L} C_i \mu_0 Q_i \tag{3.18}$$

Combing $Q_i \approx C_i(V_G - V_T)$,

$$g_D = \frac{g_{D0}}{1 + R_{sd} g_{D0}} = \frac{\left(W/L\right)\mu_0 C_i (V_G - V_T)}{1 + R_{SD}\left[\left(W/L\right)\mu_0 C_i (V_G - V_T)\right]} \tag{3.19}$$

Reminding the expression $I_D = g_D V_D$, we have:

$$I_D = g_D \times V_D = \frac{W}{L} C_i (V_G - V_T) \frac{\mu_0}{1 + R_{sd} (W/L) \mu_0 C_i (V_G - V_T)} \times V_D \tag{3.20}$$

Comparing Eq. 3.20 with Eq. 3.16, we will find that:

$$\mu_{eff} = \frac{\mu_0}{1 + R_{sd} (W/L) \mu_0 C_i (V_G - V_T)} = \frac{\mu_0}{1 + \theta^* \times (V_G - V_T)} \tag{3.21}$$

Here,

$$\theta^* = \frac{W}{L} \mu_0 C_i \times R_{sd} \tag{3.22}$$

If θ^* is known, the contact resistance can be accordingly calculated. Taking into account the phonon scattering and surface roughness impact, another part of θ_0 should be added. Hence the overall θ becomes:

$$\theta = \theta_0 + \theta^* = \theta_0 + \left(W/L\right)\mu_0 C_i \times R_{sd} \tag{3.23}$$

which replaces θ^* in Eq. 21.

To distinguish the different impacts on mobility attenuation, especially to obtain the exact contact resistance contribution and thus to accurately evaluate the contact resistance value, a transconductance parameter $G_m=(W/L)\mu_0 C_i$ is defined. Because G_m depends on the channel dimension, one can plot θ with respect to G_m if we have several transistors of diverse channel widths and lengths, as shown in Fig. 3.6. Normally, a linear variation could be obtained. The intercept to the theta axis is the contribution originating from phonon and surface roughness impact and this value is generally very small (see example later) compared to the effective value resulting from contact resistance. Hence this small θ_0 is often disregarded and contact resistance can be directly calculated from the evaluated theta, since the plot of $(1/g_m^{1/2})$ versus gate voltage in strong accumulation exhibits a linear variation (see example later).

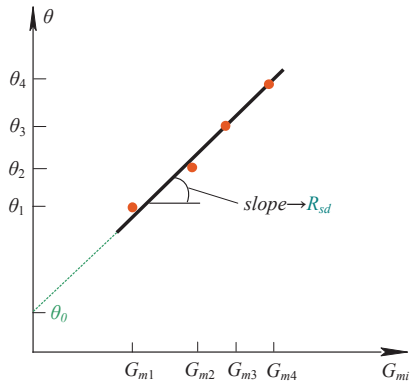


Figure 3.6 | Illustration of the linear variation of the mobility attenuation factor with respect to the transconductance parameter, where the intercept to the theta axis is the contribution from phonon scattering and surface roughness.

Sometimes, a small negative θ_0 is obtained and it might be due to the gate-voltage enhanced mobility[2] which compensates for the conventional mobility attenuation. This impact is greater in OFETs with poorer crystal structure, where the hopping transport within localized states is sensitive to the Fermi level, and thus to the gate voltage.

So, the transconductance g_m becomes:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{W}{L} C_i V_D \frac{\mu_0}{[1+\theta(V_G - V_T)]^2} \tag{3.24}$$

Y function is then defined as:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_i \mu_0 V_D} \times (V_G - V_T) \tag{3.25}$$

If we plot Y function against V_G, as shown in Fig. 3.7, one will find that the Y function is independent of the contact resistance, even though the contact resistance is included in the starting point of Eq. 3.16. This is an important feature to evaluate the intrinsic performance of organic transistors.[1] Now we summarize the extracted parameters:

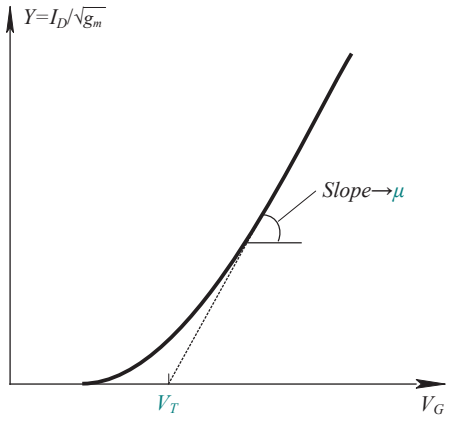


Figure 3.7 | Illustration of Y function versus gate voltage.

■■ **Low-field mobility:** μ_0

$$\mu_0 = \frac{slope}{(W/L)C_i V_D} \tag{3.26}$$

■■ **Threshold voltage:** V_T, as seen the intercept of the fitting straight line of Y function in the V_G axis.

■■ **Mobility attenuation factor:** θ, by manually fitting from the $(1/g_m^{1/2})$ versus gate voltage in strong accumulation, where a linear variation can be observed.

■■ **Contact resistance:** R_{sd} (if θ_0 is negligible)

$$R_{sd} = \frac{\theta}{(W/L)C_i\mu_0} \tag{3.27}$$

One should note that, the contact resistance obtained here is in individual transistors, in contrast to the one provided by the transfer-line method (TLM) which necessitates several transistors of diverse channel lengths, the result is only an average value for the whole set of transistors.

3.3 SPLIT C-V

In the above discussion, the C_i is assumed to be the theoretical value calculated by the equation below:

$$C_i = \frac{\varepsilon_i}{t_i} \tag{3.28}$$

where ε_i and t_i are the permittivity and the thickness of the gate insulator, respectively. In reality, the two parameters may differ from the technologically pre-defined value, especially the insulator thickness. This deviation causes some errors in other parameters evaluation: e.g. mobility, threshold voltage and contact resistance, hence it should be accurately extracted.

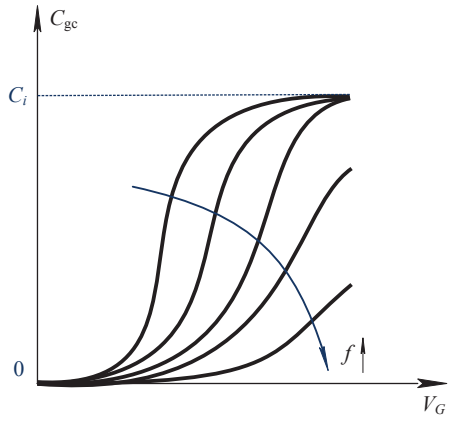


Figure 3.8 | Illustration of the C-V characteristics measured by split C-V technique.

The capacitance-voltage (C-V) characteristics are the basic transistors electrical properties and could be measured by either quasi-static C-V or split C-V technique. The difference between them resides in the applied test frequency. If this frequency is so small that could be regarded as a DC signal, this is seen as quasi-static C-V measurement. It usually includes the feedback charge method and the linear ramp method. In the latter, the tested capacitor is pre-charged to a specific DC voltage in a limited period, and then a current of the opposite polarity is forced to discharge the capacitor. Because $C=\mathrm{d}Q/\mathrm{d}V$ and the charge $Q=\int I\mathrm{d}t$, with a specific ramp rate the charge variation rate and thus the capacitance at various voltages can be calculated. This quasi-static C-V technique is useful for OFETs[5, 8] because if OFETs' mobility is very small no response will be detected by split C-V. However, this quasi-DC C-V technique is sometimes impeded by the small current variation, limited voltage range and the large gate leakage in OFETs, the split C-V is thus more commonly used.

By split C-V method, the capacitance between the gate and source-drain (denoted as C_{gc}) and the capacitance between the gate and the substrate (denoted as C_{gb}) can be measured. This technique was first developed for the characterization on the interface trapped charge density and the substrate doping density in silicon MOSFETs, and next was applied to the effective mobility analysis.[9] Due to the thin-film structure in OFETs, only the C_{gc} is measured in which the source-drain electrodes link together and connect to the low point of the capacitance bridge, and the gate electrode connects to the high point. Sweeping the biasing voltage, a small AC signal (such as sine waveform) is superimposed to DC bias in order to detected the charge variation with respect to the small AC signal, hence the capacitance of C_{gc} can be calculated for each bias, as seen in Fig. 3.8.

One can see that a plateau at high gate voltages is formed, indicating the channel formation. The height of that plateau corresponds to the C_i. Alternatively, the unit surface charge density in the channel Q_i can be obtained by integration as:

$$Q_i = \int_{-\infty}^{V_G} C_{gc}(V)dV \tag{3.29}$$

where the lower limit (here $-\infty$) is for the gate voltage at which C_{gc}=0. This charge Q_i can be directly used to analyze the effective mobility instead the charge approximation $Q_i \approx C_i(V_G - V_T)$.

Note that, if the frequency of the applied AC signal is increased, the measured C-V characteristics may show a stretch-out or a substantial decrease, as seen in Fig. 3.8. The former is known due to the interface states since more states can response to the AC signal at low frequencies, and thus the corresponding capacitance is higher.[10] That's why this C-V measurement is often implemented at high frequency to avoid the interface traps impact in silicon MOSFETs, e.g. at 100kHz-1MHz. However, such frequencies might be too high for organic transistors, because at high frequency the carriers of low mobility will not have enough time to diffuse from contacts into the channel. Hence the accumulation channel cannot response to the AC signal and in turn contributes to the C-V characteristics. In any rate, the converging curves at low frequencies offer an accurate C_i but give an overestimated Q_i since not only mobile carriers but also the trapped ones (at the OSC/dielectric interface and/or in the OSC bulk) contribute to such a C-V property. This effect will be discussed in detail later.

Till now, three main methods have been presented and the principal parameters can be evaluated. Nevertheless, they are not enough to deeply describe the OFETs characteristics, for instance, the free carrier mobility in OSC or OFETs might be substantially different from the extracted ones. Therefore, in the next section we separately address the mobility and contact resistance evaluation with illustration of some experimental results.

3.4 MOBILITY CHARACTERIZATIONS

There are several methods to obtain the free carrier mobility, in particular the Hall Effect measurement.

■ Hall Effect mobility

Hall Effect measurement is a very important tool to observe the intrinsic free carrier mobility without the influences arising from traps, contact resistance and gate/drain voltage dependences etc. Another unique feature is that it could directly measure the free carrier density because the trapped carriers cannot contribute to the Hall voltage as the Lorentz force, relying on the carrier velocity, becomes zero for these trapped carriers. Certainly it can distinguish the n-type or p-type conduction, alike its usual use.

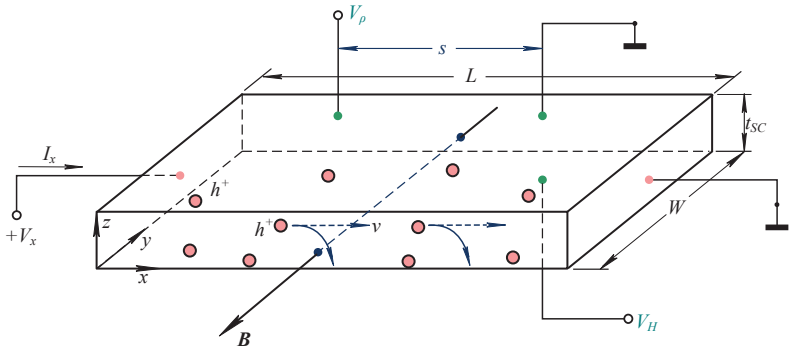


Figure 3.9 | Illustration of Hall Effect measurement in a transistor. Assuming the conduction is by holes, and they are moving from left to right under a lateral electrical field. At the same time, a magnetic field *B* is applied from the back to front side. The Lorentz force drives the holes deviating from its originally horizontal path and moving downwards to the bottom. Hence there will be a potential drop between the up/bottom sides of this semiconductor, V_H. In this case, an illustrated positive V_H should be detected.

Fig. 3.9 shows the set-up for Hall Effect measurement, here only the holes conduction is considered. As a positive voltage is applied to the left side with respect to the right side, holes drift along x direction with a velocity v. Due to the magnetic field ($-y$ direction), the holes experience a downward Lorentz force ($F_Z=qv\times B$) and move to the bottom of this semiconductor, a built-in positive charge at the bottom surface will induce a built-in electrical field E_H, corresponding to a potential drop defined between up/bottom sides, Hall voltage $V_H(=E_H t_{SC})$ with t_{SC} being the semiconductor thickness. As more charge carriers are accumulated, a steady state will attain at which the Lorentz force balances the columbic force induced by the built-in Hall field. Thus we have:

$$q\cdot(V_H / t_{SC})+qv\times B=0 \tag{3.30}$$

It will become:

$$V_H / t_{SC}=v_x B \tag{3.31}$$

As the hole drift velocity corresponds to the external current I_x as:

$$v_x=\frac{J_x}{qn}=\frac{I_x}{(qn)(Wt_{SC})} \tag{3.32}$$

where n is the mobile hole concentration, W is the channel width. Combing Eqs. 3.30 and 3.31, we obtain:

$$V_H=\frac{I_x B}{qnW} \tag{3.33}$$

From another point of view, the mobile holes concentration can be known according to the measured Hall voltage as:

$$n=\frac{I_x B}{qWV_H} \tag{3.34}$$

To derive the Hall mobility, basing on the drift current expression:

$$J_x=qnu_H E_x \tag{3.35}$$

where μ_H is the Hall Effect mobility, E_x is the lateral electrical field and it equals to $E_x=V_x/L$ with L being the channel length, we have:

$$\frac{I_x}{Wt_{SC}}=qnu_H\frac{V_x}{L} \tag{3.36}$$

and thereby,

$$u_H=\frac{I_x L}{enV_x Wt_{SC}} \tag{3.37}$$

In Fig. 3.9, if there is another probe which detects the potential drop along x direction V_ρ with distance s from the Hall voltage measurement probe, one can calculate the bulk resistivity as:

$$V_\rho=I_x\rho\frac{s}{Wt_{SC}}\Rightarrow\rho=\frac{V_\rho}{I_x}\frac{Wt_{SC}}{s} \tag{3.38}$$

This resistivity is often used to Hall Effect mobility derivation.

3.5 CONTACT RESISTANCE CHARACTERIZATIONS

■ **Transfer-line method (TLM)** *(based on the manuscript published in Appl. Phys. Lett., 97, 063302, 2010)*[11]

TLM is also called transmission-line method, or sometimes, transfer-length method, is widely used for organic field-effect transistors (OFETs) contact resistance evaluation.[12-17] This method was first developed to estimate the contact resistance value of amorphous silicon thin-film transistors.[18] It necessitates several transistors of various channel lengths and provides the average contact resistance value of the whole set of studied transistors. Unfortunately, large parameters variation usually existing in OFETs, such as mobility and threshold voltage, severely limits the TLM application. The main issues concern the large deviation of extracted contact

resistance values, in particular at small gate voltages[12] and for the OFETs having only a few channel lengths. In some extreme cases, the TLM cannot be used due to excessive parameters dispersion. Actually, such difficulties can be overcome by a simple modification of the TLM equation as will be discussed below.

In this section, we first discuss the root causes of the conventional TLM (C-TLM) drawbacks i.e. large channel resistance variations and related difficulties for application. Taking into account these problems, a modified TLM (M-TLM) is proposed and applied to two groups of OFETs (p-type and n-type). Then, by comparing the results obtained from C-TLM and M-TLM, we investigate by simulation the error that could occur in the two TLM extractions.

The applied organic devices are fabricated on gold-plated 125μm-thick polyethylene-naphtalate (PEN), using a top gate structure for both n and p-type devices.[19] The 30nm gold layer is patterned by photolithography with a line/space resolution down to 5μm, forming the source and drain electrodes as well as the 1st level of interconnection lines between gates. N-type organic semiconductor (perylene diimide derivative) is deposited in solution by direct printing methods, defining patterns corresponding to individual devices and annealed under ambient atmosphere at 100°C, leading to a final thickness in the range of 50-200nm. P-type organic

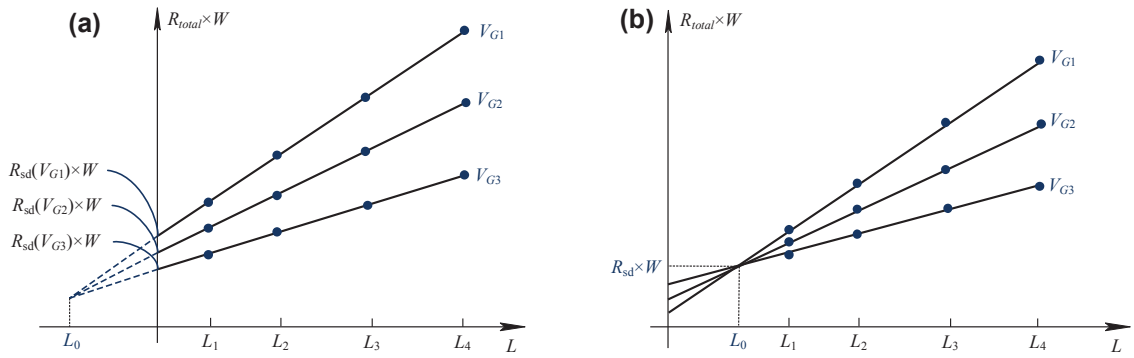


Figure 3.10 | Illustration of TLM extraction, where a crossing point is obtained and it locates on the left (a) and right (b) side of the total resistance axis. For the situation of (a), the intercepts of the fitting straight lines in the total resistance axis are the channel width normalized contact resistance, which varies with the gate voltage. For the situation of (b), the crossing point gives a gate-voltage independent contact resistance.

semiconductor (poly-triarylamine derivative) is then deposited by the same method and annealed, with a final thickness also in the 50-200nm range. The gate dielectric polymer is printed on the top of both semiconductors and then annealed, leaving open areas for via holes, with a final thickness of 1μm. Finally, a silver-ink conductor is printed on the top of dielectric and annealed at 100°C, forming in the same step the gate electrodes for devices and the 2nd level for interconnection.

The current-voltage (I-V) characteristics were measured by HP 4155. The studied OFETs exhibited good field-effect transistors behaviors. In the output characteristics, non-linear phenomena at small drain voltage were not observed, i.e. the contacts are nearly ohmic. The transfer characteristics in linear regime were used for the TLM analysis. At the same time, we detected very weak gate leakage (below 10^{-7}A/cm^2), which ensures the validity of the following TLM process.

In linear regime, the channel could be approximately regarded as a uniform resistance controlled by the gate voltage. Hence the channel resistance reads $R_{channel}=L/W\mu C_i(V_G-V_T)$, where μ is the mobility.

Due to the access or contact resistance located between the contacts and the channel, the total resistance R_{total} should be complemented by an additional term R_{sd}, such that $R_{total}=R_{channel}+R_{sd}$. The total resistance is usually normalized by the channel width W in order to become universal for devices with different W. Thus we have:[18]

$$R_{total} \times W = \frac{L}{\mu C_i (V_G - V_T)} + R_{sd} \times W \tag{3.39}$$

If we plot $R_{total}\times W$ as a function of channel length L, as shown in Fig. 3.10, we can see that: **i**) at a constant V_G, the set of $R_{total}\times W$ values of various transistors exhibit a linear variation. The intercept to the y-axis (i.e. L=0) gives $R_{sd}\times W$. At different V_G, that intercept varies with V_G, thus providing the gate-voltage dependent contact resistance $R_{sd}(V_G)$. [12, 15, 18] **ii**) The slopes of the linear regression allow us to analyze the gate-voltage dependent mobility $\mu(V_G)$.[20, 21] **iii**) The group of the fitting lines will converge towards a point at which a characteristic length from technological aspects is defined as l_0.[5, 12, 18, 22] If the fitting lines converge on the left side of the axis of $R_{total}\times W$, it is a normal TLM and the negative l_0 means that the channel length is increased. Sometimes, a positive l_0 is obtained, as seen in Fig. 3.10b. In this case, the intercepts are meaningless and a gate-voltage independent contact resistance can be extracted, and the channel length shortens as compared to the technology length.[5, 20] It should be noted that the uncertainty on the slopes of linear regression directly alters the accuracy of subsequently extracted contact resistances.

As well known, the parameters variation in organic transistors is very large, especially in polymer OFETs. Here the dispersion in μ, C_i and V_T will cause the deviation of the linear fitting slopes and more importantly of the y-axis intercept, i.e. $R_{sd}(V_G)$. Therefore, there are two possibilities we often encounter: **i**) at small V_G, e.g. around threshold, the effect of parameters variation is very pronounced. Hence the slopes vary significantly so that extracted contact resistance from intercept is not reliable. That's why the reported TLM results are mainly applied at high V_G.[12, 16] **ii**) For the OFETs with few channel lengths, particularly short channel lengths, the channel resistance does not scale sufficiently to dominate the slope variations, and thus to provide a reliable contact resistance.

However, as will be shown below, such difficulties can be overcome by the following modification of C-TLM, i.e. by dividing by L both sides of Eq. 3.39. Thus it reads:

$$\frac{R_{total} \times W}{L} = \frac{1}{\mu C_i (V_G - V_T)} + (R_{sd} \times W)\frac{1}{L} \tag{3.40}$$

In Eq. 3.39, the lack of accuracy is due to the linear fitting slopes, which comprise several parameters of the channel resistance contribution. According to Eq. 3.40, if we plot $(R_{total}\times W)/L$ with respect to $1/L$, the slope is now controlled by the contact resistance contribution $R_{sd}\times W$, which generally manifests small variation from device to device. Therefore, the linear fittings show less scattering, and the contact resistance could be more reliably obtained from this more stable fitting. Following this idea, we have extracted the contact resistance from our p-type and n-type OFETs. In the latter, the parameters variation was found to be very large, and there were only four available channel lengths as well.

A C-TLM linear fitting at a small V_G=−10V and V_G=−50V are plotted in Figs. 3.11(a) and 3.11(c), for a set of p-type OFETs. We can see that the slope is not well controlled by the OFETs with long L, the slope is disturbed by the OFETs of short L, in which the total resistance might be dominated by the contact resistance. In contrast, when using M-TLM plot, as seen in Figs. 3.11(b,d), the slope is well controlled by the OFETs of short L, where more dominant contact resistance gives a better linear fitting. Hence, the extracted contact resistance should be more reliable.

The M-TLM at various V_G is performed, as shown in Fig. 3.12(a). The extracted contact resistance is illustrated in Fig. 3.12(b) by blue circles. For the sake of comparison, the results obtained by C-TLM are also plotted in Fig. 3.12(b) by red squares. One can find small difference at high V_G, however, large difference occurs at small V_G, as discussed previously.

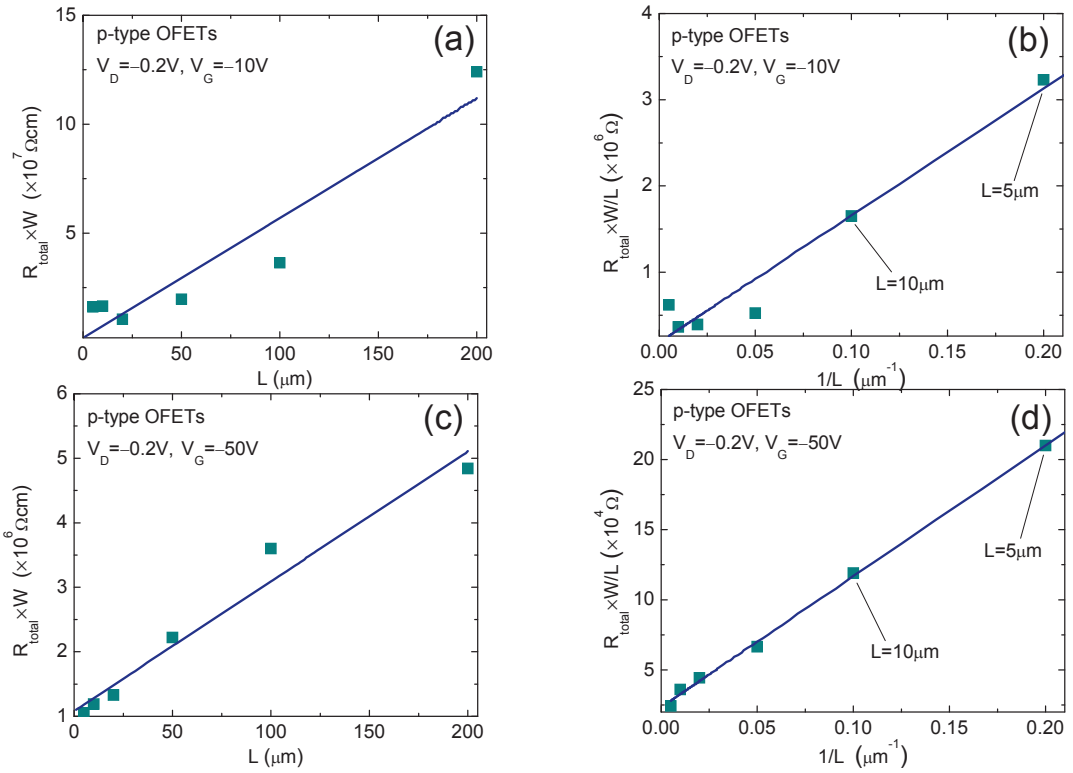


Figure 3.11 | A conventional TLM plot (a) and modified TLM plot (b) for a set of p-type OFETs, at V_G=–10V. In the modified TLM plot, the two OFETs of small channel length are indicated. They control essentially the fitting slope. At V_G=–50V, the conventional TLM (c) and modified TLM (d) are applied to the same set of OFETs. Similar results could be recognized.

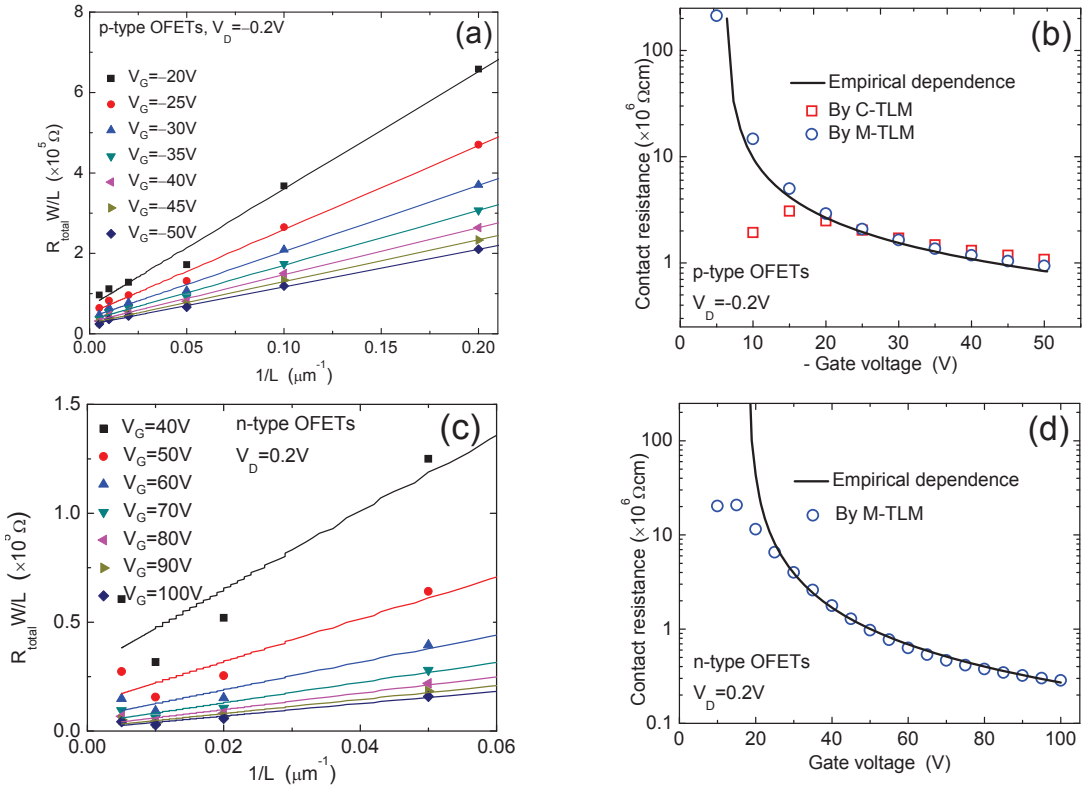


Figure 3.12 | The complete M-TLM for a set of p-type OFETs, at V_G from –20V to –50V. (b) The contact resistance extracted by C-TLM and M-TLM, the empirical gate-voltage dependence is indicated by black curve. (c) and (d) are the same process alike previous two figures applied to a set of n-type OFETs, with V_G from 40V to 100V. The C-TLM cannot be applied, so its results are not shown.

The gate-voltage dependent contact resistance was observed, and a number of analogous results have been reported.[15, 23, 24] As indicated in Fig. 3.12(b) by solid curve, it satisfies well the empirical dependence $R_{sd}(V_G)= R_{sd0}(|V_G- V_0|)^{-\beta}$,[25] where R_{sd0}, V_0 and β are fitting parameters. R_{sd0} represents the intrinsic contact resistance level at $V_G-V_0=1$V, V_0 denotes the gate voltage at which the channel begins to conduct below threshold, and β characterizes the gate voltage dependence of the contact resistance. Here $R_{sd0}=4\times10^7$ Ωcm, $V_0=-6.8$V, $\beta=1$ for that set of p-type OFETs.

Similarly, the two TLMs are applied to the n-type OFETs. Owing to the parameter variation and just four channel lengths, the C-TLM cannot be applied, principally showing large variation and negative contact resistance values. However, the M-TLM is still able to work, as seen in Fig. 3.12(c). The extracted contact resistance is shown in Fig. 3.12(d) by blue circles, and it also follows very well the empirical gate-voltage dependence, illustrated by solid curve. Here, $R_{sd0}=1.3\times10^8$ Ωcm, $V_0=17.8$V, $\beta=1.4$ for this set of n-type OFETs.

Furthermore, we investigated theoretically the extraction error from C-TLM and M-TLM. To this end, the following configurations were employed. There are 15 p-type OFETs; L is varying from 20μm to 200μm with uniform interval, and $W=2000$μm. Their characteristics are similar to the p-type OFETs analyzed above. The parameters variation is only in μ and V_T, and they follow the standard normal distribution. Their statistical data analysis provides the following mean value and standard deviation: $\mu=0.035\text{cm}^2/\text{Vs}$, $\sigma_\mu=0.01\text{cm}^2/\text{Vs}$, and $V_T=-9$V, $\sigma_{VT}=1$V. The other parameters, such as C_i and R_{sd}, are kept constant. Here $C_i=1.5\times10^{-9}$ F/cm^2 and $R_{sd}=2\times10^8|[V_G-(-6.8)]|^{-1}\Omega$, R_{sd} is not W normalized here since we fix $W=2000$μm. V_G is varied from −15V to −60V with step of −5V, and the drain voltage $V_D=-1$V.

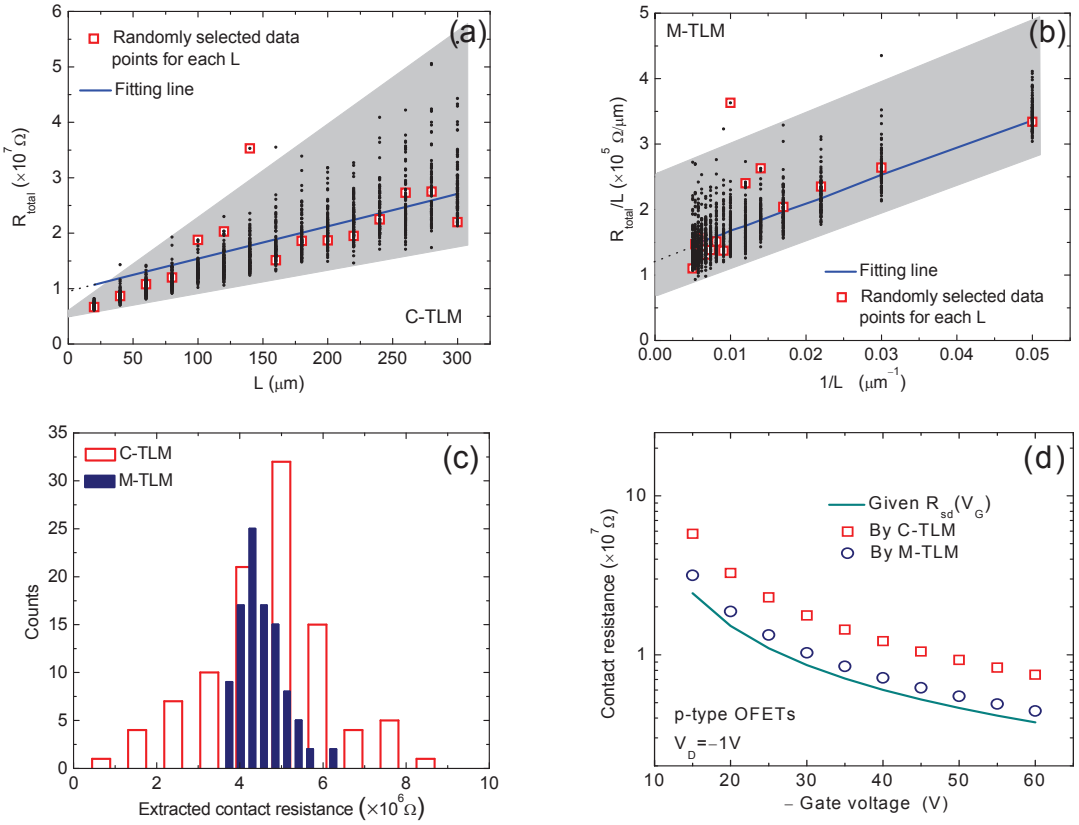


Figure 3.13 | (a) and (b) is the linear regression of the random selected data points, for C-TLM and M-TLM extraction respectively. Here the V_G is fixed at –50V and $R_{sd}(V_G=-50\text{V})=4.63\times10^6\Omega$. The shaded region indicates the data dispersion region. (c) Histogram of 100 random extractions for the two TLM extractions. (d) An example of the contact resistances extracted by C-TLM and M-TLM, by using randomly generated mobility and threshold voltage. For comparison, the previously known contact resistance is shown by green curve.

We first discuss the R_{sd} extraction at a fixed V_G=−50V. For each transistor, one hundred total resistances are randomly generated, according to the above Gaussian distribution of μ and V_T, as shown by black points in Fig. 3.13(a) and Fig. 3.13(b) for C-TLM and M-TLM extraction respectively. In C-TLM, the data dispersion or error is amplified in large L transistors. To reach the best fitting, the error should be weighted, with less weight for large L. The standard linear regression (blue line) of the randomly selected data points (red squares), however, doesn't weight, resulting in inaccurate extraction of the intercept (=$4.97\times10^6\Omega$), which represents the contact resistance. In contrast, in M-TLM the variation is in the intercept, while the slope (=$4.59\times10^6\Omega$) represents the contact resistance. Here $R_{sd}(V_G$=−50V)=$4.63\times10^6\Omega$, hence the standard linear regression will give more accurate extraction of the slope with the random data points.

The histogram of all the 100 combinations is shown in Fig. 3.13(c). We can see that the two extractions exhibit Gaussian distribution with a peak around the given R_{sd}, for this V_G=−50V. However, the relative standard deviation in M-TLM (14%) is much smaller than that in C-TLM (33%). Moreover, the error analyses for the two TLMs have been performed at various V_G. A typical example is shown in Fig. 3.13(d), and one can readily see that the M-TLM displays smaller deviation, as expected. This simulation clearly demonstrates the advantage of the M-TLM over the C-TLM.

■ **Power transfer-length method (P-TLM)** *(based on the paper published in Organic Electronics, **12**, 2019-2024, 2011)*[26]

The transfer-length method (TLM), is widely used for the contact resistance evaluation in organic field-effect transistors (OFETs).[12, 14, 15, 17] The basic principle of TLM is that, in ***linear*** regime the channel resistance (R_{ch}) is proportional to the channel length L, whereas the contact resistance (R_{sd}=R_s+R_d) does not scale with L, R_s and R_d being the source and drain access resistance, respectively. Thus, R_{sd} can be extracted from the y-axis intercepts at zero L or the converging point[5] in the plot of channel width (W) normalized total resistance (R_{tot}=R_{ch}+R_{sd}) with respect to L, for a set of transistors having various L and non-uniform W. In the case of contact resistance taken at zero L intercepts, its gate-voltage dependence can be observed by varying the gate voltages (V_G). To improve the extraction stability and accuracy, a modified version has been proposed in our previous work,[11] the modified-TLM, which can be applied at small gate voltages and in a set of transistors with few L. However, one may wonder how the contact resistance changes with drain voltage (V_D)? This can be achieved using the Kelvin probe force microscopy (KFM), by which the electrostatic potential along the channel and thus the drops at source/drain electrode can be detected.[27] The source/drain access resistance can be calculated by dividing the corresponding contact potential drop by the simultaneously measured drain current (I_D), regardless of gradual channel or not. Another alternative method is the gated four-point-probe (gFFP) measurement,[28] which generally necessitates the linear operation assumption and suffers from the channel non-uniformity. Hence, an improved gFFP was presented by Richards *et al.*,[29] and it has been implemented even into saturation regime. Nevertheless, these two techniques are a little sophisticated to be applied for device parametric test as compared to the conventional current-voltage (I-V) characterization. Moreover, on should note that the tip/probe measures the potential at the free surface of the organic semiconductor (OSC) film and not at active channel/dielectric interface, implying systematic errors.[30] Therefore, in this letter we propose a TLM based on the dissipated power in the whole device, namely the Power TLM (P-TLM), which allows the evaluation of the contact resistance in linear region as well as in saturation regime, by means of usual I-V measurements. Thus, one can investigate the contact resistance not only with respect to gate bias but also drain voltage.

Two types of transistors are employed in this work. One is the top-gate (TG, based on silver ink) and bottom-contact (BC, gold) poly-triarylamine (PTAA) OFETs made by solution-base

printing,[11] where the OSC film thickness is 50-200nm and the dielectric(Cytop^{TM}) thickness is 1μm, corresponding to the unit area capacitance C_i=1.5×10^{-9} F/cm^2. The mobility (μ) is about 0.035cm^2/Vs and threshold voltage (V_T) is around −9V. Another type is the vacuum evaporated pentacene (50nm thick) OFETs, with bottom-gate (BG, silicon) and top-contact (TC, Cu)/BC (Au/MoO_3) configurations, [25] where C_i≈8×10^{-8}F/cm^2(50nm SiO_2), μ≈0.3-0.4cm^2/Vs(TC)/0.04-0.1cm^2/Vs(BC) and V_T≈−2V-0.7V(TC)/0.7V-2.3V(BC). All devices are measured under a standard probe station at room temperature by a semiconductor parameter analyzer HP4155. More details on device fabrication can be found in the given references.

The Power-TLM relies on the fact that the total power dissipated P_{tot} in the whole device volume can be calculated, according to Joule's law as: [31]

$$P_{tot} = \int_{\Omega} \rho J^2 d\Omega \tag{3.41}$$

where ρ and J are the local resistivity and current density, respectively. The advantage of using Eq. 3.41 for evaluating the dissipated power is that it is independent of the specific conductor shape and thus of the current flow distribution. Therefore, one can separately evaluate the power dissipated in each region of the device i.e. contact and channel regions such as,

$$P_{tot} = P_s + P_{ch} + P_d \tag{3.42}$$

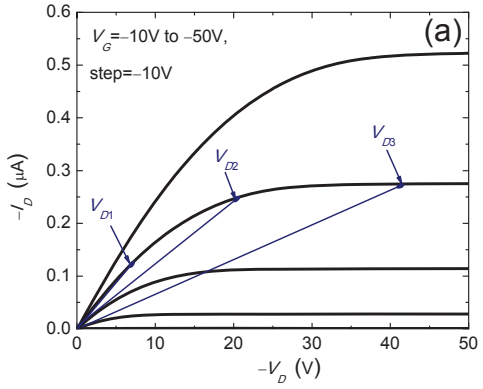
where P_s, P_d and P_{ch} are the power contribution coming from source, drain and channel regions, respectively. So, for a given drain current I_D circulating in the device, one can calculate an equivalent total resistance by normalizing Eq. 3.42 as,

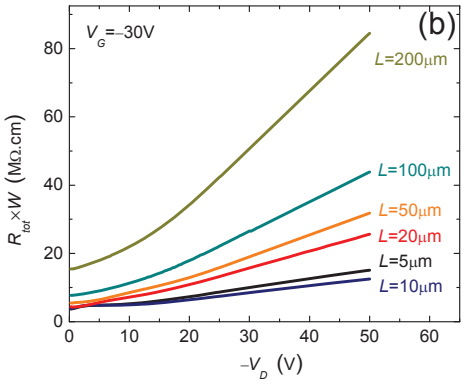
$$R_{tot} \equiv \frac{P_{tot}}{I_D^2} = \frac{V_D}{I_D} = \frac{P_s}{I_D^2} + \frac{P_{ch}}{I_D^2} + \frac{P_d}{I_D^2} = R_s + R_{chEq} + R_d \tag{3.43}$$

where R_{chEq} is the channel equivalent resistance. In the absence of contact resistance (R_{sd}=0), it would simply be equal to V_D/I_D and, by turn, scales as (L/W). In the presence of contact resistances, the channel power reads P_{ch}=$V_{Deff}I_D$, where V_{Deff} is the effective drain voltage applied to the channel, we have R_{chEq}=V_{Deff}/I_D. As I_D is governed by the effective gate (V_{Geff}) and drain voltages, hence one can simply denote I_D=(W/L)F(V_{Geff},V_{Deff}) with F being the intrinsic transistor characteristics per unit aspect ratio. Therefore, R_{chEq}=(L/W)[V_{Deff}/F(V_{Geff}, V_{Deff})]. In other words, R_{chEq} of different transistors always varies ~(L/W), for the same gate and drain biasing.

In linear regime, the channel can be regarded as a linear resistance R_{ch}=$L/[W\mu C_i(V_G-V_T)]$. In this case, Eq. 3.43 is nothing but the base of the conventional TLM since the total output resistance is a linear superposition of channel and contact resistance, i.e., R_{tot}=R_s+R_{ch}+R_d, where the unique channel length dependent contribution is R_{ch}~(L/W).

In non-linear regime, the channel cannot be treated as a linear resistance but could be still equivalent to R_{chEq}=P_{ch}/I_D^2 also scaling as ~(L/W), as discussed above. Therefore, one can find that Eq. 3.43 is a universal expression for power TLM (P-TLM): R_{chEq} varies as L/W but R_{sd} only follows ~(1/W), irrespective of linear/saturation operation. Hence R_{sd} can be extracted from the plot of the W normalized R_{tot} with respect to L, if the channel width is not uniform in the transistors' group, similar to the conventional TLM.





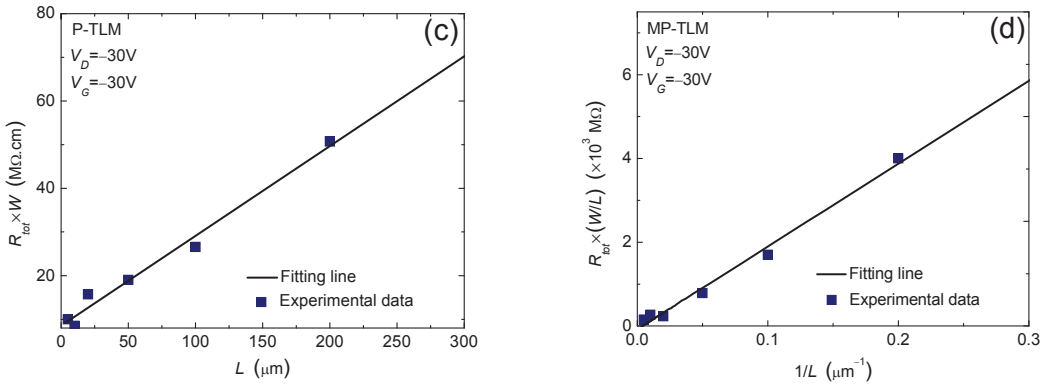


Figure 3.14 | (a) Output characteristics of a PTAA OFET (W=1000μm, L=100μm), where three data points at various V_D are chosen to illustrate the output resistance ($R_{tot}=V_D/I_D$, represented by the reciprocal of the straight lines' slope) variation versus V_D, as shown in (b), for a set of transistors with various L. (c) and (d) are the P-TLM and the MP-TLM extraction, respectively, at a fixed V_G and V_D.

Fig. 3.14a shows typical output characteristics for a PTAA OFET. At small V_D, the $R_{tot}(=V_D/I_D)$ represented by the reciprocal of the slope of illustrated straight lines is constant, indicating the ohmic operation. As V_D is increased over the limit of $V_{Dsat}=(V_G-V_T)$, the normalized $R_{tot}\times W$ increases also with V_D, as shown in Fig. 3.14b for a set of devices with various L and at fixed V_G=−30V. Fig. 3.14c clearly shows that these $R_{tot}\times W$ (at V_D=−30V) exhibit a linear variation with respect to L, providing $R_{sd}\times W$ in the y-axis intercept. However, we frequently encounter difficulties in applying P-TLM, mainly obtaining negative $R_{sd}\times W$. This is due to the parameter variation from transistors-to-transistor, e.g. μ, C_i and V_T, and it is even amplified in saturation regime and in longer channel devices.[11] Hence the modified-power TLM (MP-TLM) becomes useful, $R_{tot}\times W/L$ are plotted as a function of $1/L$, $R_{sd}\times W$ is evaluated from the slope of the fitting line rather than the intercept.[11] Fig. 3.14d shows the MP-TLM for the same extraction seen in Fig. 3.14c, one can readily find a better linear regression, implying greater accuracy.

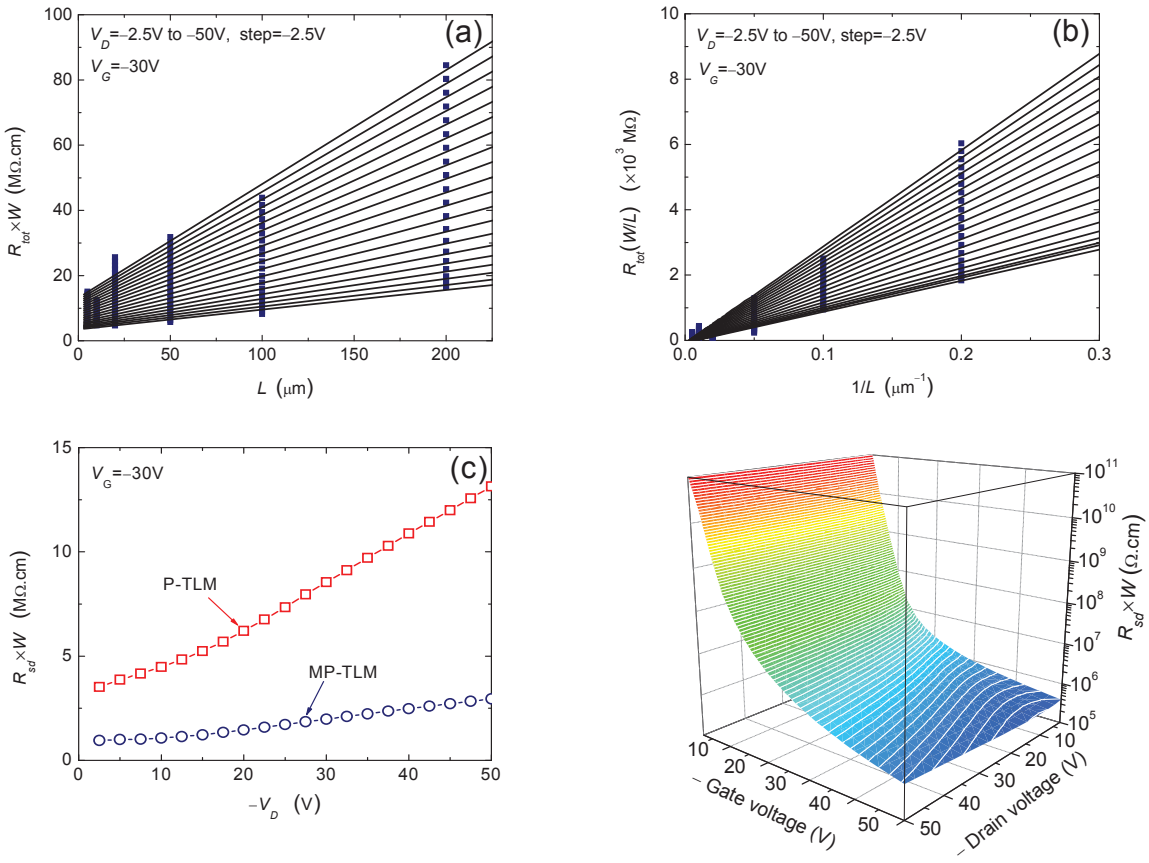
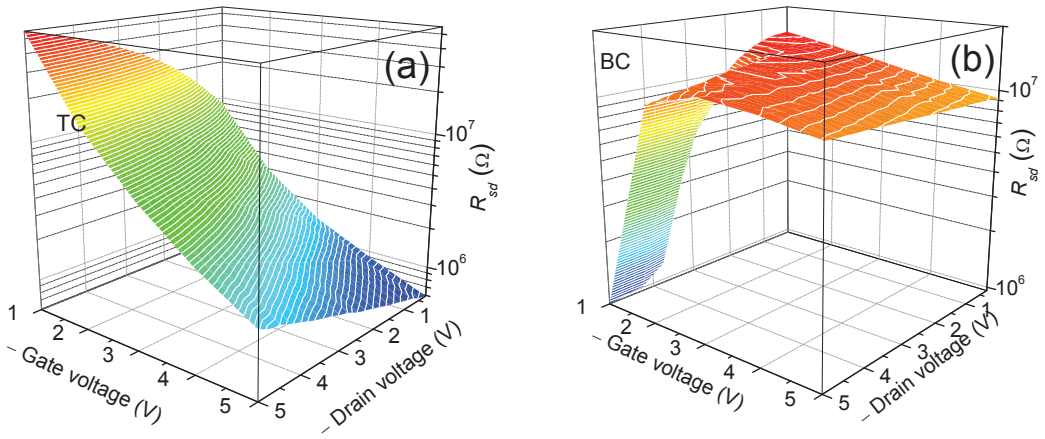


Figure 3.15 | (a) and (b) are P-TLM and MP-TLM extractions for the above PTAA OFETs, respectively, at various drain voltages and at fixed V_G=–30V. (c) shows the extracted results by the two power TLMs. (d) are the global contact resistance extracted by MP-TLM, at various V_G and V_D.

The two power TLM extractions are applied at various V_D, as shown in Figs. 3.15a and 3.15b. The obtained $R_{sd}\times W$ is shown in Fig. 3.15c. Note that the contact resistance represented by the intercepts in y-axis (P-TLM) or the slopes (MP-TLM) for this transistors' group of linear fitting lines remain constant at small V_D and afterward increases with V_D. The former constant $R_{sd}\times W$ in linear regime is reasonable because the small drain voltage doesn't significantly affect the source and drain access resistance. However, as V_D is much increased, the channel will be pinch-off on the drain side and thereby, R_d increases with V_D while R_s remains the same.[23, 29] One may notice the large deviation between the results obtained by the two power-TLMs, as seen in Fig. 3.15c. In view of the greater accuracy and higher stability of MP-TLM, it is preferred for the next analysis. The overall $R_{sd}\times W$ (at various V_D and V_G) are shown in Fig. 3.15d, strong gate-voltage dependence and relatively weak drain-voltage dependence can be observed.

Next, the same procedure is applied on two groups of pentacene OFETs (bottom-gate and uniform W=500μm). The evaluated R_{sd} is shown in Figs 3.16a and 3.16b, for TC and BC group, respectively. Compared to BC counterparts (cf. Fig. 3.16c), the TC OFETs show much stronger gate-voltage dependence, consistently with the literature.[24, 25, 29, 32] In staggered transistors (e.g. BG/TC OFETs here), carriers must traverse the entire semiconductor film in the contact region where the bulk conductivity strongly depends on the carrier density modulated by the gate voltage. This bulk resistance dominates the overall contact resistance, manifesting a strong gate-voltage dependence.[16, 29, 32] In coplanar devices (e.g. BG/BC OFETs here), the channel directly connects the two electrodes. Thus R_{sd} is predominantly controlled by the contribution in a low conductive access region in the immediate vicinity of the contacts, in which a large number of defects reside in.[1, 23, 30] Such a defect-rich access region is sometimes characterized as a depletion area at negative gate biases. Its width is varied by V_G, leading to an R_{sd} gate-voltage dependence.[1] However, its variation range is much smaller than for the bulk resistance (dominant component in TC OFETs) and hence, the BC contact resistances is greater than those for TC devices at higher gate voltages, in line with our previous results.[25] Note also that the TC OFETs show stronger drain-voltage dependence than BC ones, as shown in Fig. 3.16d. This is because in staggered transistors increasing V_D weakens the channel accumulation in the drain region and thus lowers the contact bulk conductivity at drain contact. This feature is not significant for coplanar devices due to the directly connected channel and/or the depletion space screening from the lateral electrical field. One may find a rapid decrease in BC R_{sd} at small V_G and high V_D (e.g. Figs. 3.16b,c), this might be due to an extraction error or could result from a significant decrease of R_{sd} at weak accumulation and in saturation regime, as reported in Ref.[23]



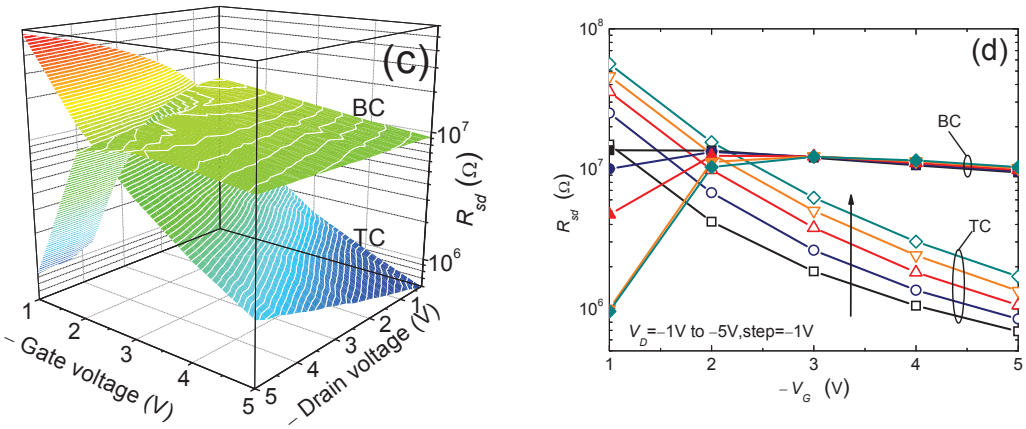


Figure 3.16 | Contact resistance obtained by MP-TLM in a set of TC (a) and BC (b) pentacene OFETs. (c) shows the comparison of the contact resistance in TC and BC group. (d) shows the gate-voltage dependence at various V_D.

In summary, a power TLM for contact resistance evaluation has been presented. It enables a complete TLM application in full range of gate and drain voltage. To ensure a more stable operation and to improve the extraction accuracy, its modified version, MP-TLM, is necessary for the extraction at small gate voltages. The contact resistance in our TG/BC (staggered) OFETs is found to be strongly attenuated with gate voltage and slightly increased with drain voltage, due to the channel pinch-off at drain contact. The results of our BG pentacene OFETs indicate that, the contact resistance in TC OFETs exhibit stronger gate and drain voltage dependences with respect to their BC counterparts. Therefore, MP-TLM is proved as a very useful tool to investigate gate and drain bias dependence of contact resistance by simple output characteristic measurements.

■ Gated four-point-probe (gFPP) technique

This technique is also widely used to evaluate the contact resistance,[28, 29, 33] its special feature resides in that it could separate the source and drain contribution to the overall contact resistance. As shown in Fig. 3.17, besides the source and drain electrodes (V_S and V_D), there are two more additional points which detect the local potential in the channel, V_1 and V_2. Suppose a gradually decreased channel potential, in which the gate voltage and the drain voltage are fixed, a linear extrapolation can be made and the potential drop on the source/drain side (ΔV_S and ΔV_D) could be calculated.

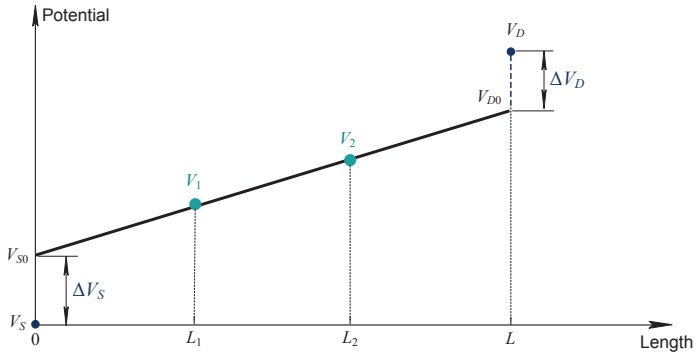


Figure 3.17 | Illustration of the gFPP technique. The two additional points detect the local potential V_1 and V_2. By a linear extrapolation, the channel potential on the source/drain side could be obtained, and thus the potential drops at

With the measured drain current, the source/drain contact resistance can be directly calculated as:

$$R_{s,d} = \frac{\Delta V_{S,D}}{I_D} \tag{3.44}$$

In order to obtain the potential drops ΔV_S and ΔV_D, one can see that for the source side:

$$\frac{V_1 - V_{S0}}{L_1} = \frac{V_2 - V_1}{L_2 - L_1} \tag{3.45}$$

As the locations of the two points (L_1 and L_2) are known in advance, hence we have:

$$V_{S0} = V_1 - \frac{V_2 - V_1}{L_2 - L_1} \times L_1 \tag{3.46}$$

The source potential drop is:

$$\Delta V_S = V_{S0} - V_S = V_1 - \frac{V_2 - V_1}{L_2 - L_1} \times L_1 - V_S \tag{3.47}$$

Similarly, we have the drain potential drop:

$$\Delta V_D = V_D - V_{D0} = V_D - \left[V_2 + \frac{V_2 - V_1}{L_2 - L_1} \times (L - L_2) \right] \tag{3.48}$$

Meanwhile, the channel potential drop can be obtained as:

$$\Delta V_{Film} = V_{D0} - V_{S0} \tag{3.49}$$

or by anther way,

$$\frac{\Delta V_{Film}}{L} = \frac{V_2 - V_1}{L_2 - L_1} \tag{3.50}$$

and thus:

$$\Delta V_{Film} = \frac{V_2 - V_1}{L_2 - L_1} \times L \tag{3.51}$$

Therefore, we could separately address the source/drain contact resistance and the channel resistance.[28] Sweeping the gate voltage, one could observe the variation of the three resistances with respect to gate voltage. The evaluation accuracy of this technique is affected by the non-uniform channel, i.e. the linear extrapolation is not accurate, thus giving misleading source/drain potential drops.

■ Kelvin probe force microscopy (KFM)

This technique is an useful method to extract the OFETs' contact resistance,[23] but it is not suitable for inorganic devices. Because large quantities of surface charge is induced by the dangling bonds often distributed at the cleaved surface of the inorganic semiconductors, e.g. single-crystal silicon. The surface charge impedes the use of potentiometry on the cross section of this kind of transistors, but in organic transistors, the weak van der Waals forces interacting among molecules free from that surface charge effect, and thus KFM is very suitable for OFETs.[27] It could also separately address the source/drain access resistance without suffering from the linear extrapolation accuracy as in gFPP measurement. Because the local electrostatic potential is measured by a non-contacted potentiometer, often having a resolution as high as 100nm,[1] the two contact potential drops as well as the exact channel local potential can be obtained. Note that the under tested OFETs can operate not only in linear regime but also in saturation regime,[29] the detected potential profile in the

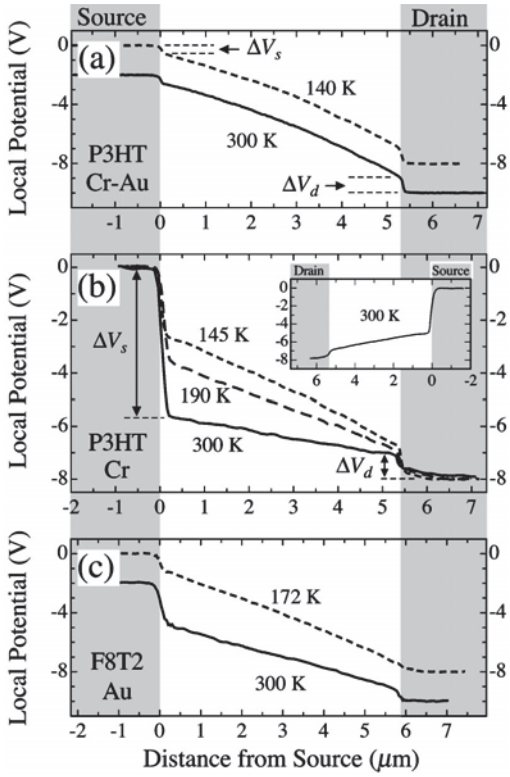


Figure 3.18 | Potential profile measured in three kinds of OFETs: (a) P3HT with contact metal of Cr-Au, channel length L=5.3μm, V_G=–20V, V_D=–8V, (b) P3HT with Cr, L=5.5μm, V_G=–40V, V_D=–8V (c) F8T2 with Au, V_G=–40V, V_D=–8V. (After Ref. [1])

channel is linear and super-linear for the two regimes, respectively. An illustration is shown in Fig. 3.18, measured in the OFETs of different organic semiconductor and diverse contact metals.

Burgi *et al.*,[27] also proposed that the conventional methods, such as the I-V characterization, evaluate the mobility from a macroscopic aspect and such a mobility is significantly limited by some extrinsic additional effects, e.g. contact resistance and the gate-voltage dependent mobility. However, the KFM offers the microscopic potential profile in the channel regardless of the above effects, which could be used to derive a more intrinsic mobility, at various gate voltages and various temperatures.

3.6 THRESHOLD VOLTAGE CHARACTERIZATIONS

As discussed in the second chapter, threshold voltage is a prerequisite for the mobility evaluation since it determines the channel charge threshold. Due to its conventional meaning is lost in OFETs, one cannot define it as the voltage at which the transistors enter from weak inversion into strong inversion and in the band diagram, corresponding to a same energy shift of Fermi level but contrary to the original side with respect to the equilibrium Fermi level. Besides the precedent threshold voltage extracted by classical method (linear/saturation regime) and Y function method, there are also numerous techniques were developed to its evaluation.

■ Turn-on voltage

In the work of Reese *et al.*,[20] the linear fits of the transfer characteristics poorly describe the OFETs' slow turn-on and pre-threshold regime,[5] the resultant threshold voltages significantly varies from 5V to −7V for a lot of devices. Hence the conventional threshold voltage is replaced by a turn-on voltage, V_{on}. It is defined as the voltage at which the mobile carriers begin to accumulate in the channel, and could be extracted from the point at which the slope of the logarithmic plot of the transfer characteristics changes sign, as shown in Fig. 3.19a.

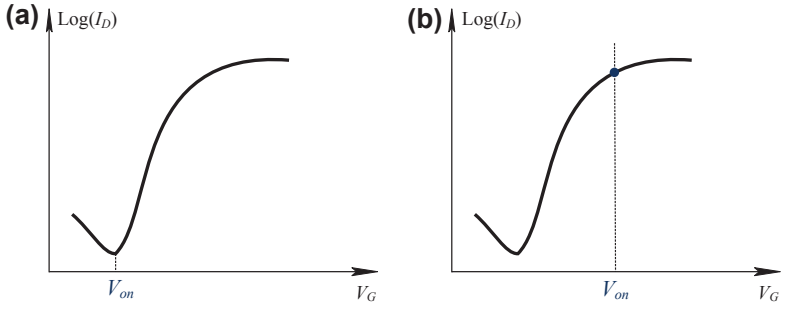


Figure 3.19 | Illustration of the extraction of the turn-on voltage from the point at which the slope of the log(I_D) changes sign (a), or the current changes from exponential to linear dependence versus the gate voltage (b).

This V_{on} exhibited much smaller dispersion compared to the linearly fitted threshold voltage,[20] not only in linear regime but also in saturation regime. Actually, the similar technique was already applied into the classical Si MOSFETs. As shown in Fig. 3.19b, the so-called turn-on voltage V_{on} is obtained from the point at which the drain current changes the gate-voltage dependence from exponential to linear. This is because in linear regime and at V_G below V_{on}, the surface potential at the OSC/dielectric interface ψ_s increases linearly with V_G and thus the drain current increases with V_G exponentially, however as V_G above this V_{on}, the ψ_s saturates, the charge and thus the drain current vary linearly with V_G. One can see a large difference in the two V_{on} and sometimes this technique is not stable,[34] hence other method is needed.

■ C-V threshold voltage

Close inspecting the I-V characterizations seen in Fig. 3.20, one will find that in linear regime (cf. Fig. 3.20a), very small current occurs at small gate voltages which reduces the ratio of I_{on}/I_{off} and increases the subthreshold slope, a super-linear increase in drain current is often observed at high gate voltages due to the gate-voltage dependent mobility, hence a linear fitting cannot be reached.

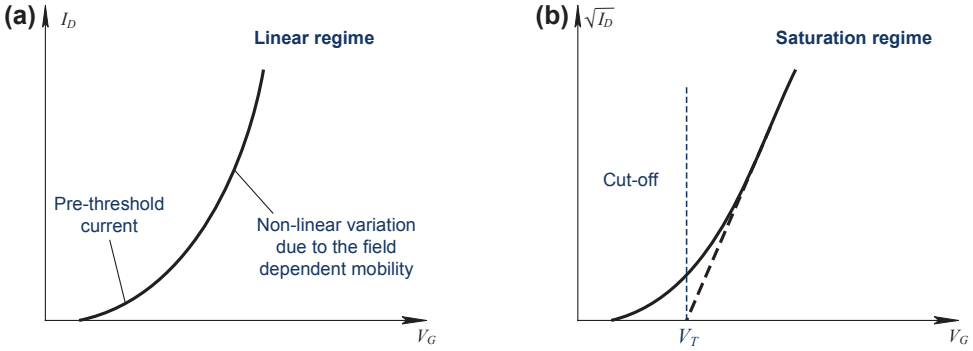


Figure 3.20 | Inspection of the difficulty in extracting the threshold voltage in linear (a) and saturation (b)

In saturation regime(cf. Fig. 3.20b), with increasing the gate voltage the transistors changes the operation mode from cut-off into a normal conducting mode, hence a linear fitting in the square root plot is easier attained relative to in linear regime. That's why this method is the most used to extract mobility and threshold voltage.

On the other hand, if we sweep the gate voltage from positive to negative (for p-type OFETs), the switch of the induced channel charges can be relatively clearly observed from the C-V characteristics, as seen in Fig. 3.21. This technique is free from the contact resistance and other parasitic resistance, as well as the field dependent mobility because the threshold voltage is extracted in the point at which an abrupt increase of C-V is observed due to the formation of carrier accumulation. This method is often sensitive to the applied AC signal frequency, thereby the quasi-static C-V is applied.[5, 8] Nevertheless, these low-frequency or quasi-static C-V may suffer from the large quantity of (slow) traps in the organic semiconductors, so this extracted threshold voltage represents a charge threshold for the traps filling rather than for the channel formation because the C-V characteristics correspond to not only the mobile charge but also the trapped charge. If the trap density is very high, the increased gate voltage induces a certain amount of charge carriers which might be completely localized by the traps (deep and shallow), an increase in C-V as shown in Fig. 3.21 will also be found. However in this case, there is no mobile charge and thus no channel formed. As a result, this C-V threshold voltage is only applicable for the cases of low trap density.

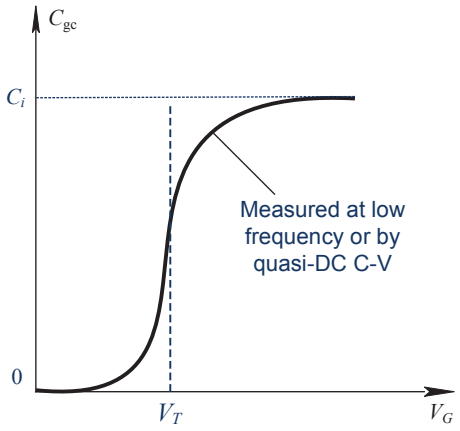


Figure 3.21 | Threshold voltage extraction by C-V characteristics.

■ Transconductance derivative threshold voltage

In addition to the extrapolated threshold voltage extracted by the transconductance (cf. Fig. 3.1), there is another way to obtain threshold voltage as shown in Fig. 3.22.

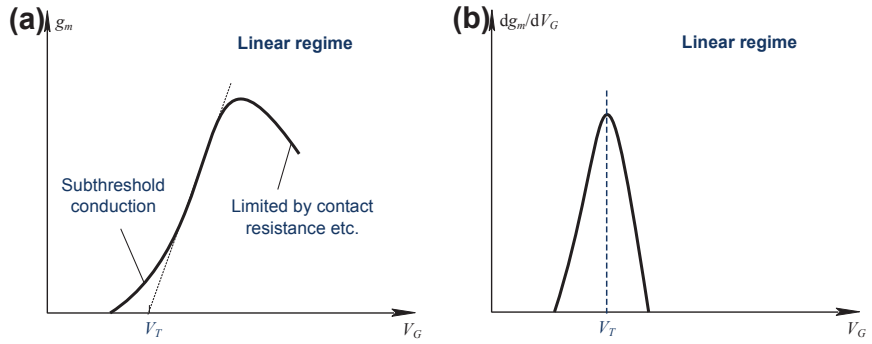


Figure 3.22 | Transconductance in extracting the threshold voltage by a direct linear fit (a) and by its derivative (b).

When $V_G<V_T$, the transconductance and thus the drain current are very small, but when $V_G>V_T$, the drain current increases linearly with V_G, as shown in Fig. 3.22a. In between there is a mutation which corresponds to the point $V_G=V_T$. This point can be clearly observed by differentiating g_m with respect to V_G, since $g_m=dI_D/dV_G$, $dg_m/dV_G=d^2I_D/dV_G^2$, a large peak will appear and it gives the V_T. This technique provides the threshold voltage without the error arising from the arbitrary selection of fitting data and free from the influences of contact resistance, drain/gate voltage dependent mobility. This method was applied to study the threshold voltage variation with respect to the drain voltage by Braga *et al.*,[35] an empirical was obtained $V_{Teff}= V_T +0.5V_D$.

Next, we will show the applications of our Y function method to two groups (TC/BC) of pentacene OFETs and address OFETs' principal parameters: mobility and contact resistance.

3.7 APPLICATION OF Y FUNCTION METHOD (*based on the paper published in Journal of Applied Physics 107, 114507, 2010*)[25]

■ A, C-V characteristics

The gate-to-channel capacitance C_{gc}-V_G was measured at various frequencies using an HP4294, with the source and drain electrodes connected to the low point of the capacitance bridge, and the gate electrode connected to its high point.

A typical C-V characteristic is shown in Fig. 3.23(a).[5] The C_{gc} increases and saturates at negative V_G, indicating the formation of an accumulation channel for p-type transistor. However, the C_{gc} substantially decreases or shifts as the applied signal frequency is increasing.[36, 37] This might be attributed to the very low mobility of organic semiconductor and/or the interfacial states. The former is usually responsible for the C-V decrease since the carriers have not enough time to diffuse from the contacts into the channel when the frequency of the applied signal is too high. Therefore the accumulation channel cannot respond to the AC signal and in turn contribute to the C-V characteristics. A large number of states at the dielectric/semiconductor interface are responsible for the C-V shift or stretch-out like in polysilicon thin film transistors (TFTs).[10].

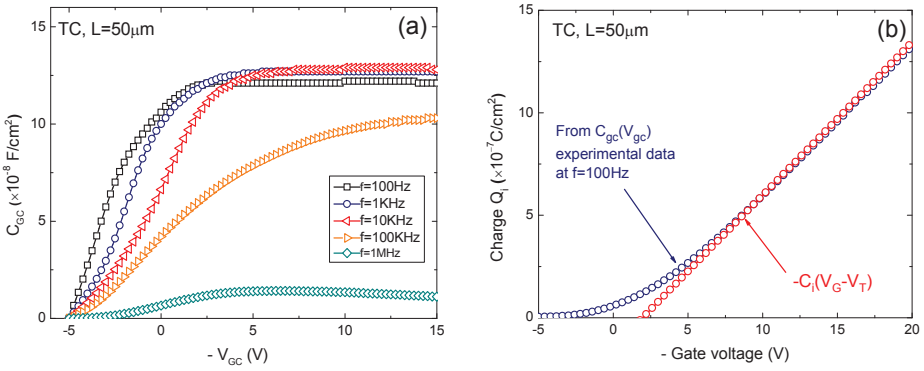


Figure 3.23 | (a) Capacitance-voltage characteristics at various frequencies for a top-contact OFET. (b) The channel charge per unit area *versus* the gate voltage for a top-contact OFET.

In spite of the abnormal characteristics behavior around threshold, the C-V curves converge towards a plateau at negative bias voltage and at low frequencies, for example lower than 1 kHz. Such converging value reveals the dielectric capacitance C_i, which will be safely used for the following parameters evaluation rather than the theoretically calculating value C_{itheo}=7.98×10^{-8} F/cm^2 (50nm S_iO_2). From Table 3.1, it is clear that the extracted C_i in BC OFETs is much less than C_{itheo}, thus avoiding an underestimation of mobility.

Similarly, the charge $Q_i(V_G)$ is obtained from the converging C-V data at low frequency (here at f=100Hz) by integrating $C_{gc}(V_G)$ with respect to V_G,[9] as shown in Fig. 3.23(b). We can see that the strong accumulation charge approximation $Q_i \approx C_i(V_G - V_T)$ is fairly close to the integrated charge from C-V data, implying the feasibility of the Y function method.

TABLE 3.1 Summary of the parameters extracted from Y function method for three TC/BC pentacene OFETs.

Transistors	W (μm)	L (μm)	C_i (F/cm^2)	μ_0 (cm^2/Vs)	V_T (V)	Theta,θ (1/V)	R_{sd} (Ωcm)
TC1	500	150	7.5×10^{-8}	0.42	-2.1	0.006	2800
TC2	500	100	9.3×10^{-8}	0.34	-1.63	0.01	3100
TC3	500	50	9.5×10^{-8}	0.36	0.71	0.023	3400
BC1	500	150	4.9×10^{-8}	0.12	0.66	0.023	5.6×10^4
BC2	500	100	4.7×10^{-8}	0.07	2.26	0.02	1.1×10^5
BC3	500	50	4.5×10^{-8}	0.04	0.81	0.06	1.6×10^5

C_i is dielectric capacitance per unit area, μ_0 is the low-field mobility, V_T is the threshold voltage, θ is the mobility attenuation factor, and R_{sd} is the access (contact) resistance.

■ B, I-V characteristics and parameter extraction

The output characteristics $I_D(V_D)$ and the transfer characteristics $I_D(V_G)$ were taken by using an HP4155. Typical output characteristic is shown in Fig. 3.24(a). Both the TC and BC OFETs exhibited good transistors behaviors during this study. The non-linear properties at small drain voltage were not observed, i.e. the contacts are nearly ohmic. We measured very slight gate leakage in these OFETs, maximum at the level of 10^{-8}A/cm^2. It ensures the validity of the following parameter extraction procedure.

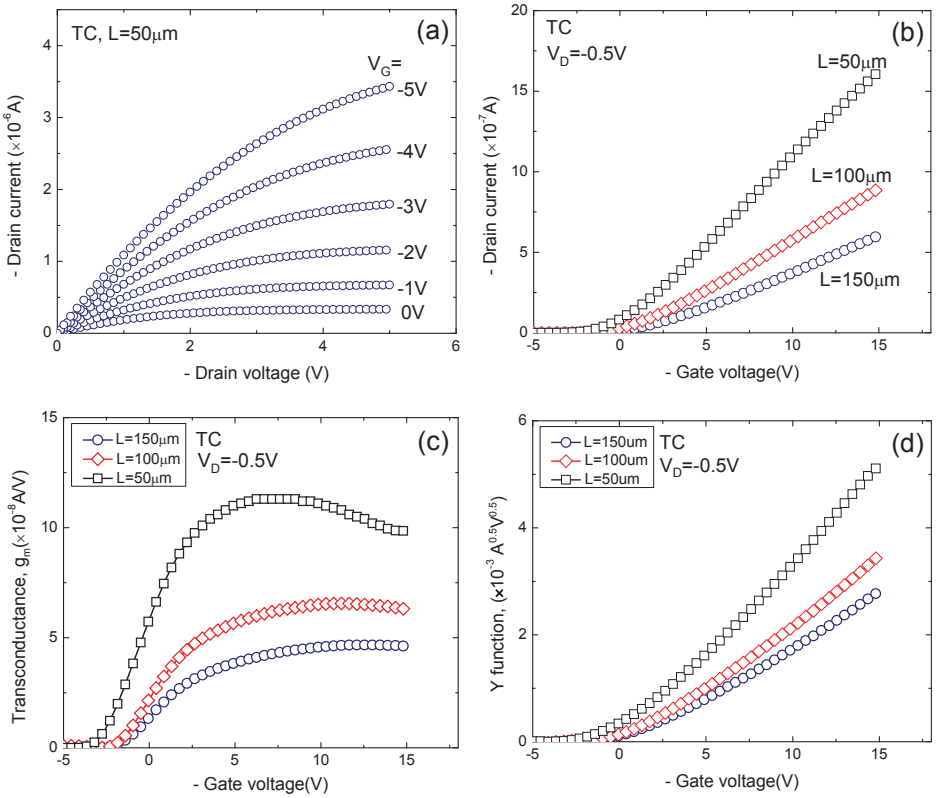


Figure 3.24 | (a) The output characteristics for a TC OFET. (b) The transfer characteristics at V_D=–0.5V of three TC OFETs. (c) The transconductance *versus* gate voltage for the three TC OFETs. (d)The Y functions plots of the three TC OFETs.

Typical transfer characteristic at small drain voltage (linear regime) is shown in Fig. 3.24(b), for three OFETs of different channel lengths. The transconductance and the Y function with respect to gate voltage are shown in Fig. 3.24(c) and Fig. 3.24(d), respectively. From Fig. 3.24(d), the plots of Y function exhibit good linearity, in agreement with its original definition. The low-field mobility and the threshold voltage are accordingly extracted from slope and intercept, respectively. As discussed above, the contact resistance could be evaluated by extracting the mobility attenuation factor, as seen in Fig. 3.25(a). The extracted parameters are summarized in Table 3.1.

With regard to the extracted low-field mobility values, μ_0, it can be stated that: **i)** The μ_0 in BC OFETs is much less than in the TC counterparts. Analogous results have been reported by Sirringhaus *et al.* [38] This difference was ascribed to the disruption of the self-organization process near the source-drain electrodes in BC configuration,[23, 39] where small grains are formed at the contact edges, as shown by the morphology results in Fig. 2.7(b). **ii)** The μ_0 decreases in BC group as the channel length scales from 150μm to 50μm. Note that, such mobility degradation of μ_0, is independent of contact resistance, which was not the case in ref.,[15] where the mobility diminution originated from the contact resistance. One possible explanation is due to the low mobility region near the contacts, which affects the overall channel mobility. Note that, this impact is larger in shorter channel transistors, whereas the same decrease was not observed in TC OFETs.

For the sake of comparison, the extracted contact resistance is normalized by the channel width. It can be noted that: **i)** Its values are around the level of 10^3Ωcm for TC OFETs and 10^4~10^5Ωcm for BC OFETs, which is several orders of magnitude higher than the state-of-the-art silicon MOSFETs,[40] where the contact resistance seldom exceeds 0.1Ωcm. Such high contact resistance will severely limit the OFETs performance if no progress will be made on this issue in the future. **ii)** Its value in BC group is one or two orders of magnitude greater than in TC devices. Similar results have been reported and there are many explanations.[17, 23, 41-43] One plausible cause is from the above mentioned contact regions, which could also lead to higher contact resistance.[1, 30] It should be noted here that the contact resistance extracted by Y function method is for individual OFETs, contrasting with the transmission-line method (TLM), by which only the average contact resistance value of the whole set of OFETs could be obtained. Therefore, the Y function method provides the possibility to directly investigate the contact resistance evolution in a single transistor; which can be very useful for the bias stress analysis.[44]

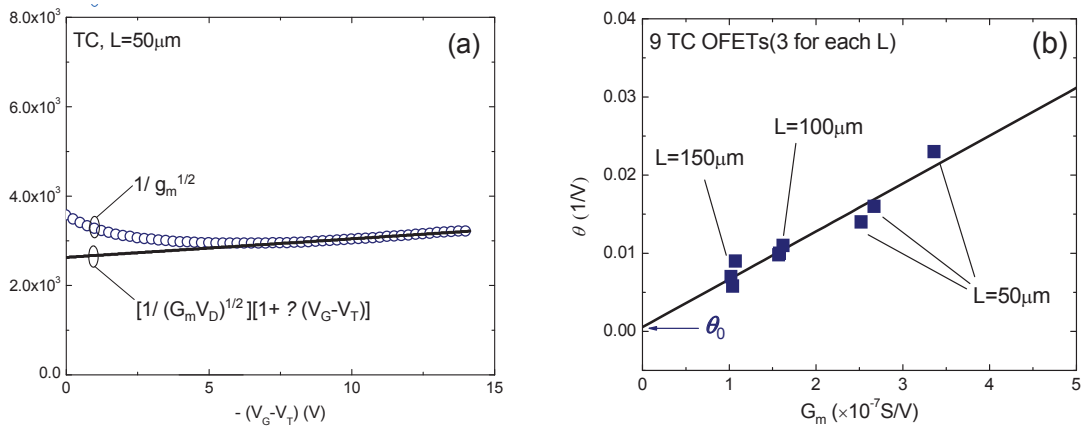


Figure 3.25 | (a) Evaluation of the mobility attenuation factor, theta, in a TC OFET. (b) Plot of the mobility attenuation factor with respect to the transconductance parameter, in nine TC OFETs.

Furthermore, with the theta values obtained in TC group, we plotted $\theta(G_m)$ in Fig. 3.25(b), according to Eq.3.23. The nine points are well located in the fitting straight line, inferring the validity of the Y function method, i.e. the mobility attenuation factor of the studied OFETs exhibits good scaling. The slope gives the contact resistance R_{sd}=3.06×10^3 Ωcm, consistent with

the value extracted directly by the Y function method. The intercept in θ axis is θ_0, here θ_0=5.5×10^{-4}1/V. Sometimes slightly negative value is obtained, and it might be due to the gate-field enhanced mobility,[45] which compensates for the conventional mobility attenuation. In any case, its value is very small compared to the effective θ values in the studied OFETs, i.e. the contact resistance contribution dominates the mobility attenuation.

■ C, Mobility analysis

The contact resistance severely affects the OFETs' electrical properties. It should be noted that, in the low frequency noise (LFN) analysis, the fluctuations from contact resistances often dominate the overall LFN at strong drain current.[46] In the DC characteristics, the drain current is also limited by the contact resistance,[1] especially in linear regime. The apparent or extrinsic mobility in organic transistors is substantially different from the intrinsic mobility in organic semiconductors, which might cause difficulty in the mobility evaluation. Thanks to the Y function, one can eliminate the contact resistance influence and obtain the intrinsic low-field mobility. At the same time, it offers us an insight into the effective mobility as well as into the field-effect mobility.

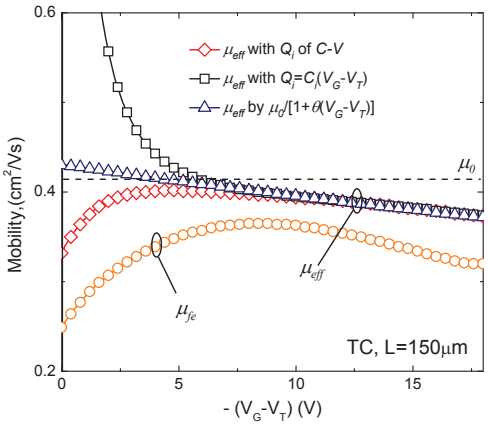


Figure 3.26 | Mobility comparison in a TC OFET, the dash line indicates the low-field mobility. For the charge from the split C-V, it was at *f*=100 Hz.

As seen in Fig. 3.26, we analyzed the low-field mobility μ_0, the effective mobility μ_{eff} and the field-effect mobility μ_{fe}. μ_0 is extracted by Y function. μ_{eff} is calculated with the charge given by split C-V or by the strong accumulation charge approximation, $Q_i \approx C_i(V_G - V_T)$, or, reconstructed from the Y function method using Eq. 3.21. The good agreement of the three μ_{eff} curves at strong accumulation confirms once again the validity of the Y function method. The μ_{fe} is obtained from the transconductance. According to the previous result shown in Fig. 3.25(b), the major effect for mobility degradation is due to the contact resistance. We can see that μ_{eff} is substantially attenuated at high gate voltage; more attenuation emerges from μ_{fe}, due to the square power in the denominator of Eq. 3.24. Large discrepancy exists between μ_0 and μ_{eff} (or μ_{fe}), and it might be larger in OFETs with shorter channels, with worse contact resistance, or, with semiconductors having higher mobility. This is due to the fact that the portion of channel resistance $R_{channel}$ in the total transistor resistance R_{total}(=$R_{channel}$+R_{sd}) decreases, leading to more contact domination. [1, 47] In contrast, the low-field mobility μ_0 is not affected by series resistance, and, thus is clearly more appropriate than μ_{fe} for the mobility evaluation in OFETs, although μ_{fe} has been widely used so far.

■ D, Comparison with TLM

In Y function method, the contact resistance is assumed constant; but it might depend on gate voltage.[16, 23] Hence the transmission-line method (TLM) analysis has also been performed to compare the results with those obtained by the Y function method. As seen in Fig. 3.27(a) and 3.27(b), the R_{sd} of several TC and BC OFETs were evaluated by TLM. Both R_{sd} of the two sets satisfy very well the empirical dependence:

$$R_{sd}(V_G) = R_{sd0}(V_G - V_0)^{-\beta} \tag{3.52}$$

where R_{sd0}, V_0 and β are fitting parameters. R_{sd0} represents the intrinsic contact resistance level at $V_G - V_0$=1V, V_0 denotes the gate voltage at which the channel begins to conduct below threshold, and β characterizes the gate voltage dependence of the contact resistance. Here R_{sd0}=2.2×10^5 Ωcm, V_0=6V, β=1.6, and R_{sd0}=5.3×10^6 Ωcm, V_0=6V, β=1.5 for the TC and BC set of OFET,

respectively. Larger R_{sd0} and smaller β are obtained in BC OFETs, as expected.[24, 29] The R_{sd} extracted by YFM in two typical OFETs (TC/BC) is illustrated by the dash line, as seen in Fig. 3.27(b). The error bar indicates that the R_{sd} values of various OFETs fall in the range of TLM results.

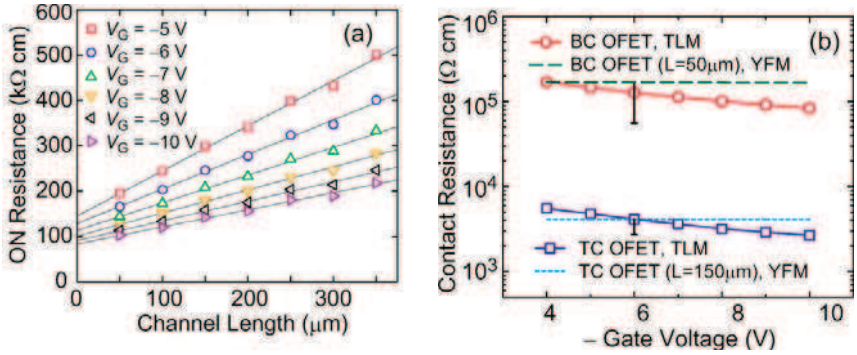


Figure 3.27 | (a) TLM results of a set of BC OFETs. (b) The contact resistances evaluated by TLM (curve) and Y function method (straight dash line) as a function of gate voltage, the error bar at the straight line represents the contact resistances of various OFETs.

The measured drain current in linear regime is then corrected from series resistance effect either by a constant R_{sd} (from YFM) or by $R_{sd}(V_G)$ (from TLM), according to the equation,

$$I_{Dcor} = \frac{I_D}{1 - \left(I_D / V_D\right) \times R_{sd}} \tag{3.53}$$

Then, the mobility values corrected from series resistance R_{sd} or $R_{sd}(V_G)$ were extracted using the same procedure, and are shown in Fig. 3.28(a) and 3.28(b), for typical TC and BC OFETs, respectively.

After the R_{sd} correction from YFM, in both TC and BC OFETs, μ_{eff} and μ_{fe} become constant and approach μ_0. This means that the mobility attenuation in the studied OFETs results principally from the contact resistance, and, that the gate-field enhanced mobility is not significant.

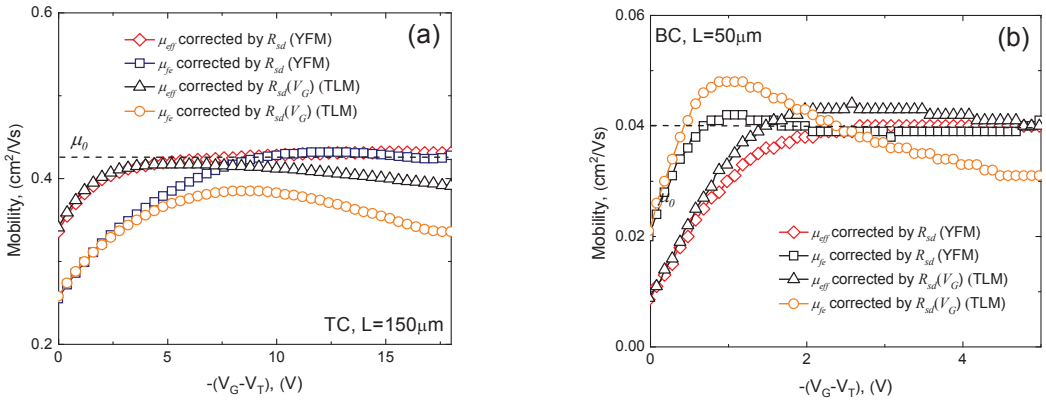


Figure 3.28 | The contact resistance corrected mobility in the TC (a) and BC (b) OFETs. For the effective mobility, the employed charge is from the split C-V data at f=100 Hz.

After the $R_{sd}(V_G)$ correction from TLM, as seen in Fig. 3.28(a), μ_{eff} and μ_{fe} still decrease at high gate voltage in the TC OFET. This phenomenon is reproducible in the other TC OFETs; hence such mobility decrease might be due to surface roughness and/or phonon additional scattering. This effect is eliminated by the overcorrection of the Y function method as the R_{sd} exceeds $R_{sd}(V_G)$ at strong accumulation, cf. Fig.3.27(b). Nevertheless, the difference is small since μ_{eff} =0.39cm^2/Vs at V_G =−15V, which is slightly less than μ_0=0.43 cm^2/Vs in that TC OFET. Similar results were observed in BC OFETs, cf. Fig.3.28(b). In other words, the Y function method is accurate enough and therefore is usable for the contact resistance evaluation despite its constant value assumption. From a practical viewpoint, a fast and accurate estimation of the contact resistance for a single transistor is usually more important than the variable

contact resistance taken from several transistors. Hence, the Y function method is worth being considered as an alternative method for the contact resistance evaluation of organic transistors.

3.8 STATIC CHARACTERIZATIONS OF PTAA OFETS

We studied four sets of PTAA OFETs (CEA-LITEN) during this thesis, their substrate code are 379, 383, 404 and 727. For clarity, only one typical transistor for each substrate is selected for results illustration and the extracted parameters are summarized in Table 3.2. Because the layout of the former three substrates (379, 383 and 404) is different from the latter one (727), thus the same transistor T4 (W=1000μm, L=80μm) on substrate 379, 383 and 404 and the OFET U10 (W=1000μm, L=20μm) on substrate 727 are chosen as examples.

■ C-V characteristics

As seen in Fig. 3.29, C-V curves decrease with test frequency like the OFETs we have studied above (e.g., pentacene OFETs).[48] It is due to the very low mobility in the organic semiconductor (PTAA here), and the carriers have not enough time to diffuse from the contacts into the channel when the frequency of the applied small AC signal is too high. The accumulation channel cannot respond to the measured AC signal and in turn, contribute to the C-V characteristics. At the same time, the C-V curves shift or stretch-out as the applied frequencies are increasing, e.g. for the OFET on substrate 404. That is because of a large number of states existing at the dielectric/semiconductor interface like in the poly-silicon thin-film-transistors (TFTs).[10]

One can clearly see that, a plateau is nearly formed at high gate voltage that is often used to extract the unit area capacitance of dielectric C_i. Owing to the strong dependence on the measured AC signal frequency, this C_i is taken at the minimum frequency (here f=100Hz). C_i varies significantly from transistor-to-transistor, irrespective of the nominal technology parameters. For instance, C_i=2×10^{-8} F/cm^2 for the OFETs on substrate 379 and 383 but it is decreased down to around 1×10^{-8} F/cm^2 for the OFET on substrate 404 and significantly increased up to 7×10^{-8} F/cm^2 for the OFET on substrate 727.

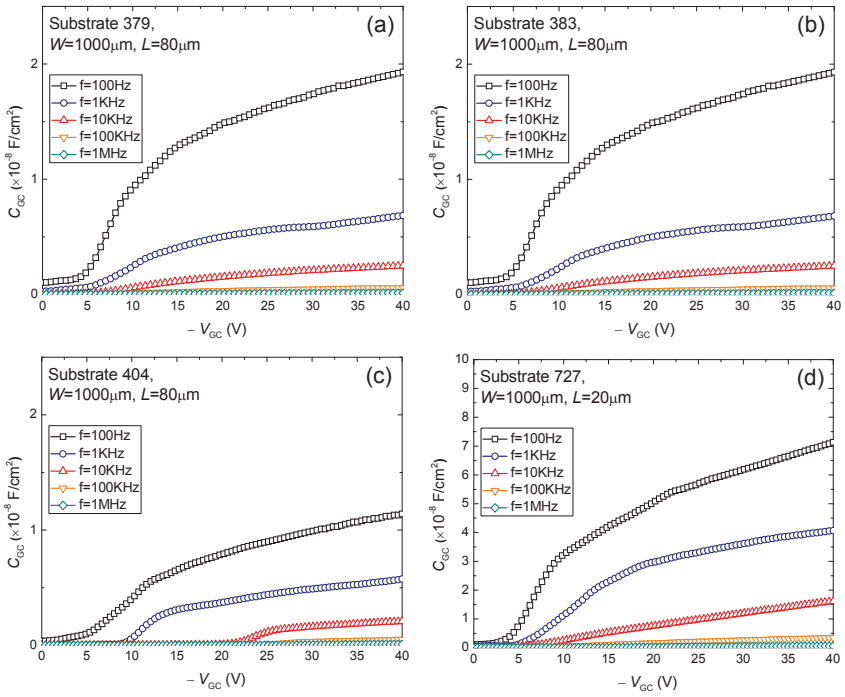


Figure 3.29 | C-V characteristics of several PTAA OFETs measured at various frequencies.

To eliminate the extrinsic effects, we firstly examined the possible issues on the measured mode, i.e. serial or parallel mode. Basing on the schema below, the impedance $Z_P(R_P, C_P)$ is measured in the parallel model to minimize the serial contact resistance effects.

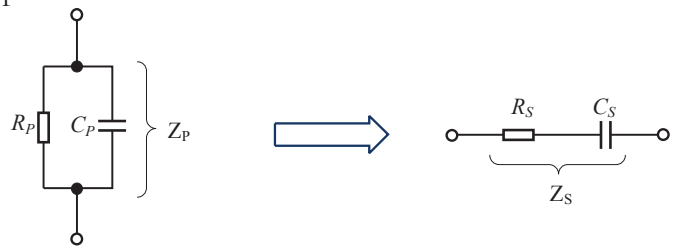


Figure 3.30 | Illustration of the impedance equivalence between the parallel/serial

This overall Z_P should be equivalent to that in serial mode $Z_S(R_S, C_S)$, as seen in the right-side illustration of the same figure. The measured (R_P, C_P) allows us to calculate the corresponding C_S, according to the relationship below:

$$C_S = \frac{1+(\omega R_P C_P)^2}{\omega^2 R_P{}^2 C_P}, \quad R_S = \frac{R_P}{1+(\omega R_P C_P)^2} \tag{3.54}$$

where $\omega=2\pi f$ is the angular frequency. Fig. 3.31 shows the calculated C-V characteristics in serial mode. It's clear that the shape of these C-V curves is not much changed but the corresponding plateau is lowered compared to the parallel mode value. Hence one can conclude that the measurement mode doesn't significantly affect the C-V characteristics.

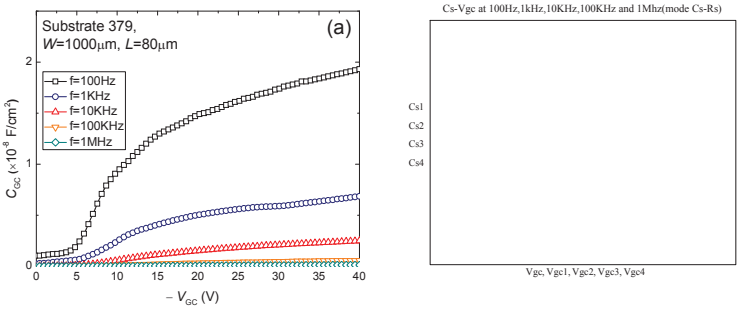


Figure 3.31 | (a) Measured C-V characteristics in parallel mode. (b) Calculated C-V characteristics in series mode(figure b update later).

Note the theoretically calculated C_{itheo}=1.48×10^{-9} F/cm^2 with ε_o=8.85×10^{-14} F/cm, ε_r=2 and t_i=1.2μm. Having this C_{itheo}, we try to compare with the experimental results since the channel area used above is $W\times L$. However, the effective area contributing to the C-V characteristics may be the total area, as the blue one seen in Fig. 3.32. So we have:

$$A_{effective} = [N_D \times L + (N_D + 1)L_D + 2\times 500]\times(W + 2\times 500) \quad (\mu m^2) \tag{3.55}$$

where N_D is the number of comb-shape channel, L is the channel length between two fingers, and L_D is the width of each finger, W is the channel width. 500μm is the distance from the border to the central area. By using this effective area, the corresponding unit area capacitance is calculated but one obtained a large deviation relative to the theoretical value; the amplitude of variation could be up to 30 times, i.e. from 1/3 to 10 times of theoretical C_{itheo}. This inconsistence implies that the effective active area responding to the C-V characteristics might be not that one in Eq. 3.55.

The simultaneously fabricated capacitance also allows us to investigate the C-V characteristics because all the technological area would give a more precise capacitance. We selected one capacitor, S2 on substrate 727 with W=50000μm and L=500μm because substrate 727 is the best one among the four sets. Its C-V results are shown in Fig. 3.33. From this figure one can clearly see that the measured capacitance at f=50Hz C_i=1.47×10^{-9}F/cm^2 (f=50Hz) is exactly equal to the theoretical C_{itheo}=1.48×10^{-9} F/cm^2. Such a good agreement suggests also that the

theoretical capacitance is applicable and that C-V at f=50Hz could be used for the charge calculation by split C-V technique.[9]

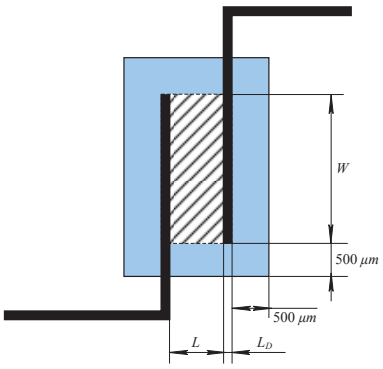


Figure 3.32 | Schema of a comb-shaped OFET with one effective channel.

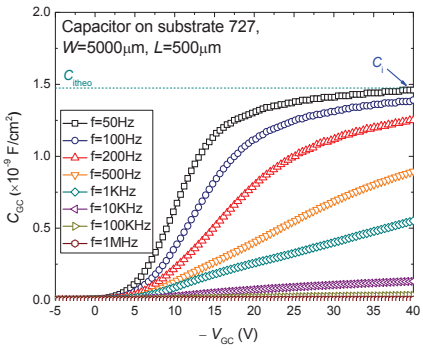


Figure 3.33 | C-V characteristics measured on a concurrently fabricated capacitor on substrate 727.

I-V characteristics

Output characteristics I_D-V_D

These OFETs generally showed good field-effect transistor behaviors but one can still find the non-linearity at small drain voltages in the OFET 383, which means the non-ohmic contacts presumably induced by the poor quality crystal structure around the contact region.

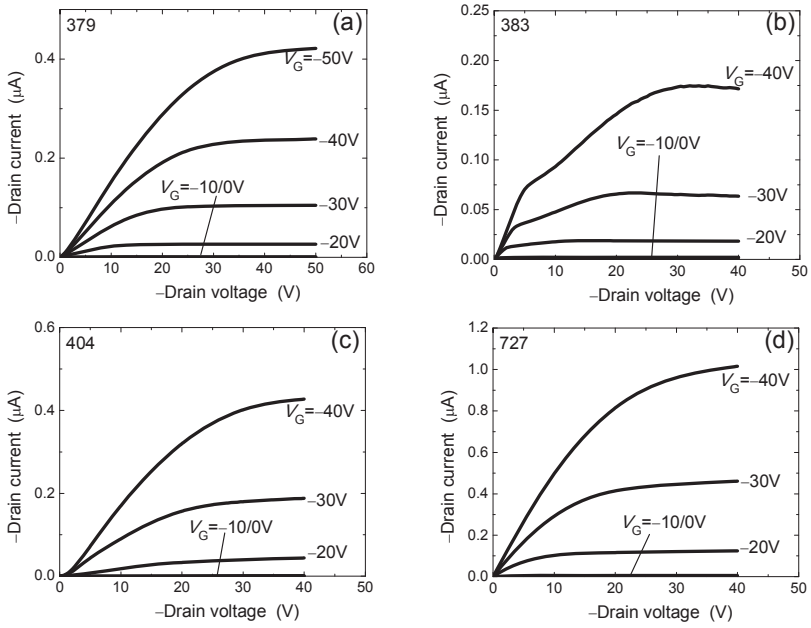
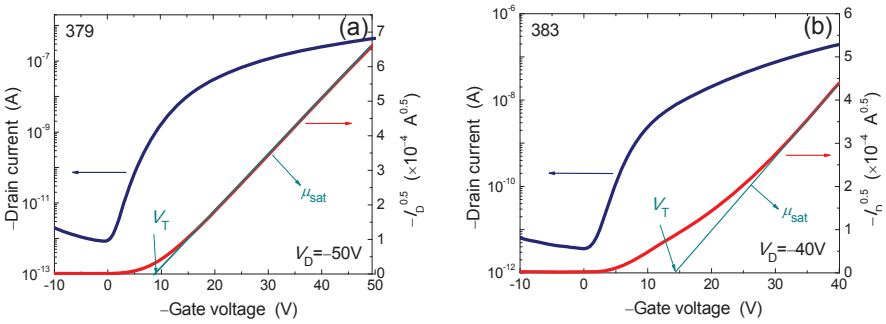


Figure 3.34 | Output characteristics of several PTAA OFETs.

Transfer characteristics I_D-V_G in saturation regime

Typical transfer characteristics in saturation regime are shown in the figures below. The square root of the drain current versus the gate voltage is used to extract the saturation field-effect mobility and the threshold voltage, as discussed above.



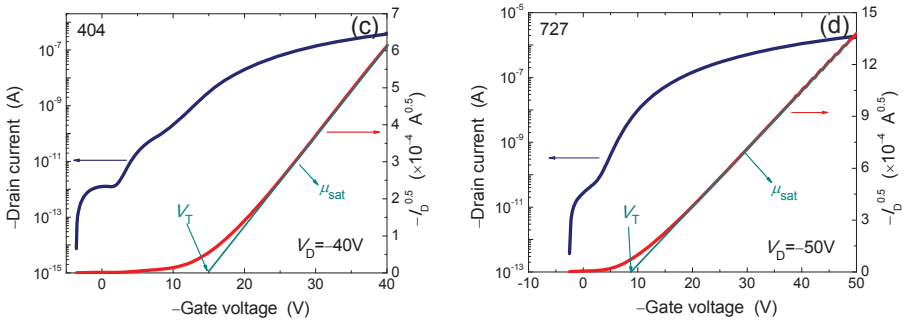


Figure 3.35 | Transfer characteristics in saturation regime of several PTAA OFETs.

However, a non-linearity in extraction (e.g. in the OFET 383), thus the evaluated mobility and threshold voltage are not reliable. This non-linearity is often found in short-channel transistors and might be due to the drain-voltage dependent mobility and/or non-ohmic contacts.

Meanwhile, one can observe the hysteresis by back and forth sweeping the gate voltage, as seen in Fig. 3.36. In general, there are two types of hysteresis: permanent and dynamic. The former could be used to make organic memory and the latter will cause difficulty in the integrated circuit design, because hysteresis sometimes significantly shifts the transistors' threshold voltage, especially in the OFETs with polymer dielectric and thus leading to faulty operation. This is due to the fact that the correct operation of functional digital and analog ICs critically depends on stable operation points for each transistor; a large shift in threshold voltage could make the actual operating point outside the predefined operation windows. If the number of integrated transistors is increased, such an impact of hysteresis will become very severe. There are numerous possible originations for hysteresis in OFETs: 1 trapping and migration of dopant; 2 traps and defects in dielectric and semiconductor; 3 mobile ions; but an explicit explanation is still not clear. In principal, hysteresis increases with temperature and strongly depends on the sweeping rate and direction. Here we performed the I-V measurements with medium sweep rate, the delay time is 50ms between two points and the step is ±0.25V. It's clear the hysteresis is quite large in the OFET 404 but becomes negligible in the OFET 727, implying their poor and high quality, respectively.

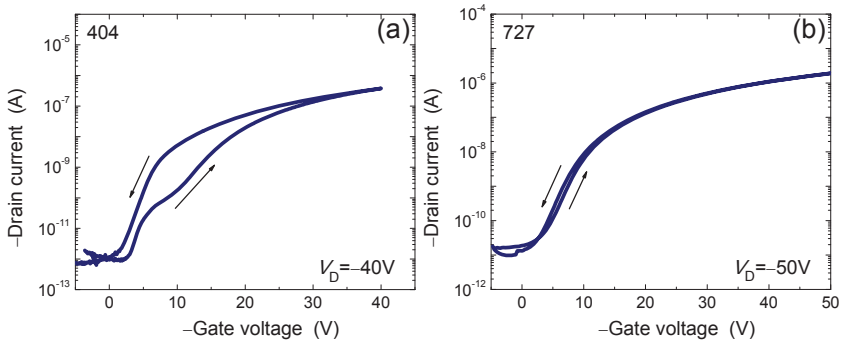
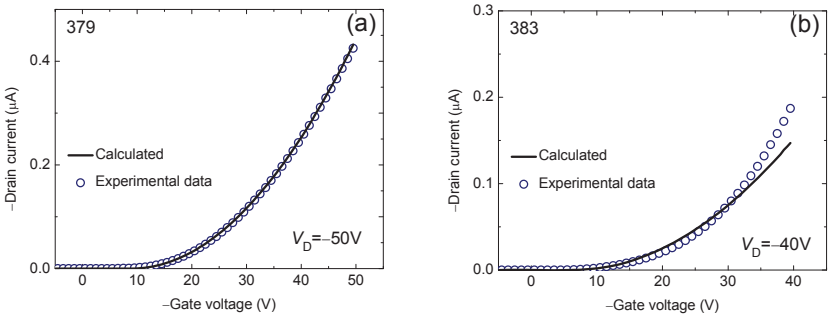


Figure 3.36 | Observation of hysteresis by back and forth sweeping the gate voltage.

With the extracted parameters, one can calculate the drain current based on Eq. 3.5. A good agreement between the experimentally measured values and the calculated ones could be readily found, except for the OFET 383 in which the large deviation is attributed to the large error in extraction due to the non-linearity seen in Fig. 3.34b.



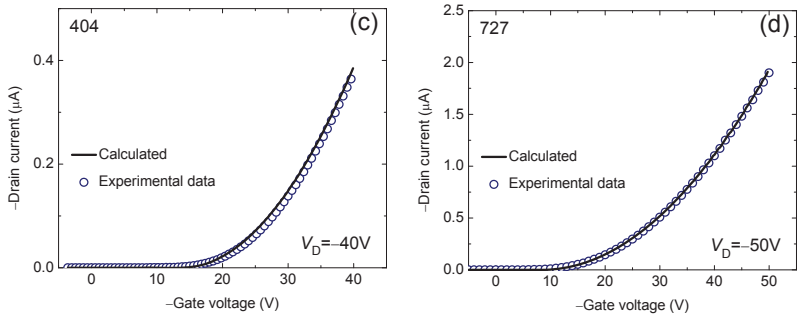


Figure 3.37 | Comparison of the drain current between the experimental data and the calculated values.

■■ *Transfer characteristics I_D-V_G in linear regime*

Typical transfer characteristics in linear regime and the corresponding transconductance are shown in the figures below. For the OFET 383 the maximum of trans-conductance g_{max} cannot be reached, the extraction of the threshold voltage is thus impossible by the conventional method (cf. Fig. 3.1). In this case, Y function method becomes necessary. So, we only concentrate on the analysis with YFM.

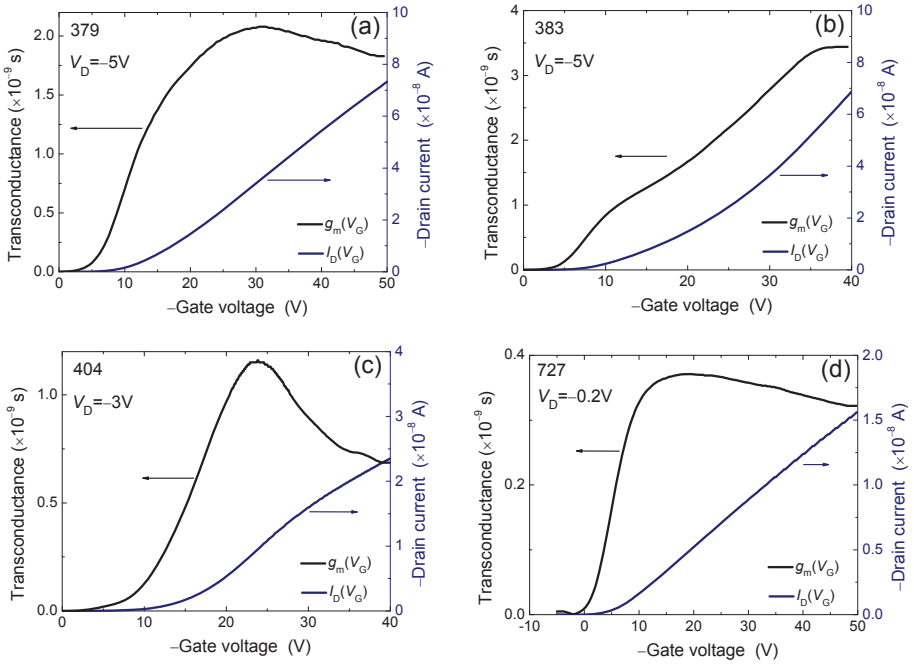
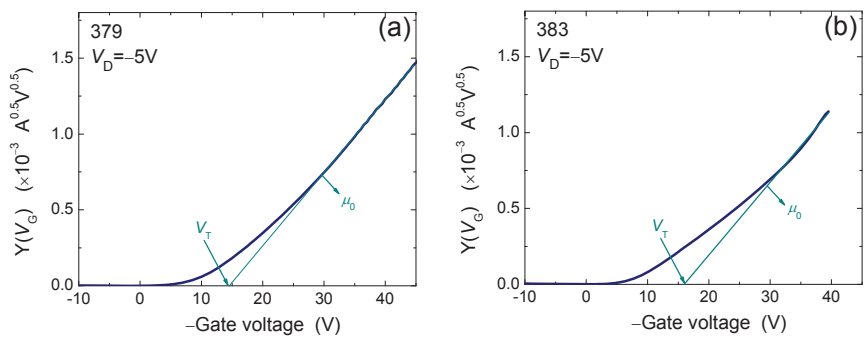


Figure 3.38 | Transfer characteristics in linear regime. The calculated transconductance is also shown in the same figure by bleu curve.

Figs. 3.39 show the Y function for the four OFETs and its slope contains the low-field mobility, μ_0, and the intercept to the V_G axis is the threshold voltage. The fairly good linearity in OFETs 379 and 727 reflects the good validity of Y function method, thus one can safely extract μ_0 and V_T. Bad results are also found in OFET 383, confirming its poor quality and several extrinsic characteristics existing in this transistor.



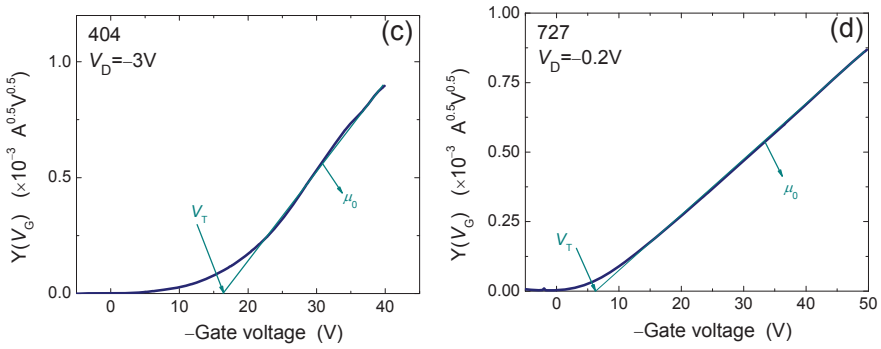


Figure 3.39 | Y functions for the four example OFETs by which the low-field mobility and the threshold voltage can be extracted.

Another advantage in using YFM is to obtain the contact resistance value in individual transistors; it could be achieved by evaluating the mobility attenuation factor θ, cf. section 3.2. With the contact resistance value, one can correct the drain current by which the corrected field-effect mobility can be obtained.[25] This analysis is shown in Fig. 3.40a for an OFET 727(here R_{sd}=1.55×10^{6}Ω, or W×R_{sd}=1.55×10^{5}Ωcm). It's clear that the contact-resistance corrected field-effect mobility is much improved in strong accumulation and becomes constant with the gate voltage. Such a constant value very approaches to that of low-field mobility which was previously extracted by Y function (μ_0=0.028cm^2/Vs), consistent with the nearly contact resistance dominated mobility attenuation in OFETs.[25] This inference is confirmed by plotting θ with respect to the transconductance parameter (G_m) in several OFETs having different channel dimension (cf. Eq. 3.23), as seen in Fig. 3.40b. The slope of the linear regression corresponds to the channel width normalized contact resistance (here W×R_{sd}=2.46×10^{5}Ωcm), close to the value directly obtained by Y function method. The relatively small value of intercept in y-axis θ_0=6.8×10^{-5} 1/V, namely the slight mobility limitation coming from phonon scattering and surface roughness impact, indicates that the overall mobility attenuation is almost resulted from contact resistance.

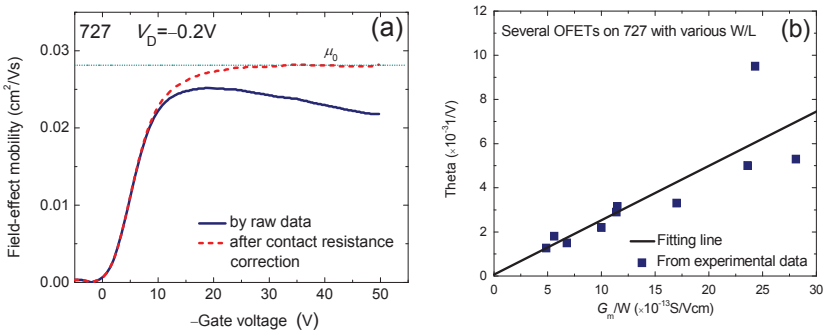


Figure 3.40 | (a) Field-effect mobility before and after contact correction. (b) The mobility attenuation factor versus the transconductance parameter for several OFETs having different W and L.

The subthreshold slope in the subthreshold region can be used for determining the surface state density N_{SS}, as shown in Fig. 3.41a. N_{SS} is evaluated as shown in Fig. 3.41b, here the minimum N_{SS}=4.11×10^{11}/eVcm^2 corresponds to the minimum subthreshold slope 2.7V/decade, similar results could be found in ref.[49]

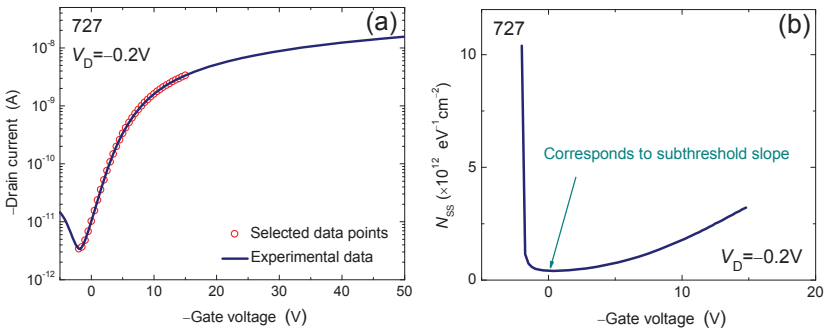


Figure 3.41 | (a) Extraction of the subthreshold slope. (b) The corresponding extraction of the surface states density.

Finally, with the extracted parameters (μ_0, V_T and θ), we compare the calculated value with the experimental data according to Eq. 3.16, as shown in Fig. 3.42. Very good agreement can be found apart from in OFET 383. In the following section and next chapter, we will see that the Y function show much greater reliability and accuracy in the mobility and threshold voltage evaluation in short-channel OFETs, especially at low temperatures.

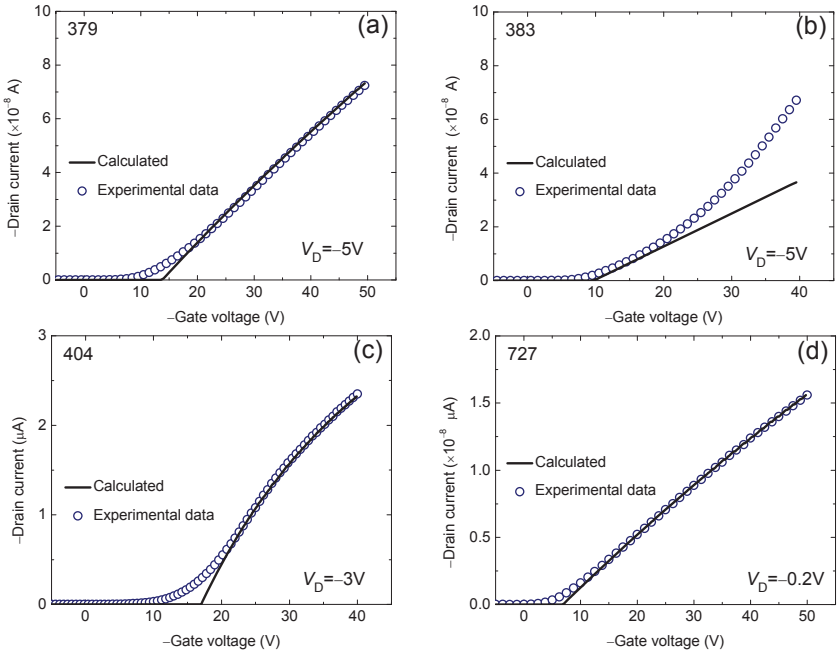


Figure 3.42 | Comparison of the experimental data with the calculated ones.

3.9 STATIC CHARACTERIZATIONS OF N-TYPE OFETS

We analyzed a set of n-type OFETs (N1400, CEA-LITEN), their substrate code is 729. For simplicity, we show the typical results only in one transistor F4 (W=3000μm, L=50μm). The C-V characteristics are shown in Fig. 3.43a, one will readily find abnormal behaviors compared to the previously studied p-type OFETs and no plateau has been attained at high gate voltages. This is due to the very high threshold voltage (up to 40V) in these transistors so that a strong channel accumulation is not formed at even the maximum available voltage for C-V measurement (40V). In this case, the theoretically calculated C_{itheo}=1.48×10^{-9} F/cm^2 is used for the next analysis. Fig. 3.43b shows the output characteristics and it exhibits normal field-effect transistor behaviors and the non-linearity at small drain voltages (i.e. non-ohmic contact) is not observed. Next, its transfer characteristics are examined for parameters extraction. In saturation regime (cf. Fig. 3.43c), at first one used a maximum gate voltage of V_{Gmax}=50V (V_D=50V) but a clear linear region in plotting the square root of the saturation drain current against the gate voltage is always unreachable. Therefore, we tried to apply a high V_{Gmax}=100V (with V_D=100V) and observed a linear region as seen in Fig. 3.43c. The threshold voltage is found to be as high as 37.3V and μ_{sat}=0.13cm^2/Vs. By back and forth sweeping V_G, one addresses hysteresis in this n-type OFET. As shown in Fig. 3.43d, it is clearly negligible, implying fairly low trap density which is then proved to be true by the subthreshold slope technique and low-frequency noise analysis. Similarly, the experimental results are compared with the calculated values, a good agreement is obtained, cf. Fig. 3.43e. Such a high V_T is further confirmed by the analysis in linear regime as shown in Fig. 3.43f, the transconductance attains a peak at very high gate voltage, thus the extrapolated threshold voltage V_{Text} should be very high (cf. Fig. 3.1). Here the Y function (Fig. 3.43g) becomes linear at V_G over 50V and the obtained V_T=45V and μ_0=0.15cm^2/Vs. With the evaluation of the mobility attenuation factor shown in Fig. 3.43h, the contact resistance is calcu-

lated, here R_{sd}=2.94×10^{5}Ω or W×R_{sd}=8.8×10^{4}Ωcm, comparable to or a little smaller than those in PTAA OFETs 727. The subthreshold slope is also analyzed (Fig. 3.43i), and the associated surface states density is found to be around N_{SS}=2.98×10^{11}/eVcm^2. Finally, the experimental data are compared with the calculated one by using the previously extracted parameters; a good agreement can be seen in Fig. 3.43j.

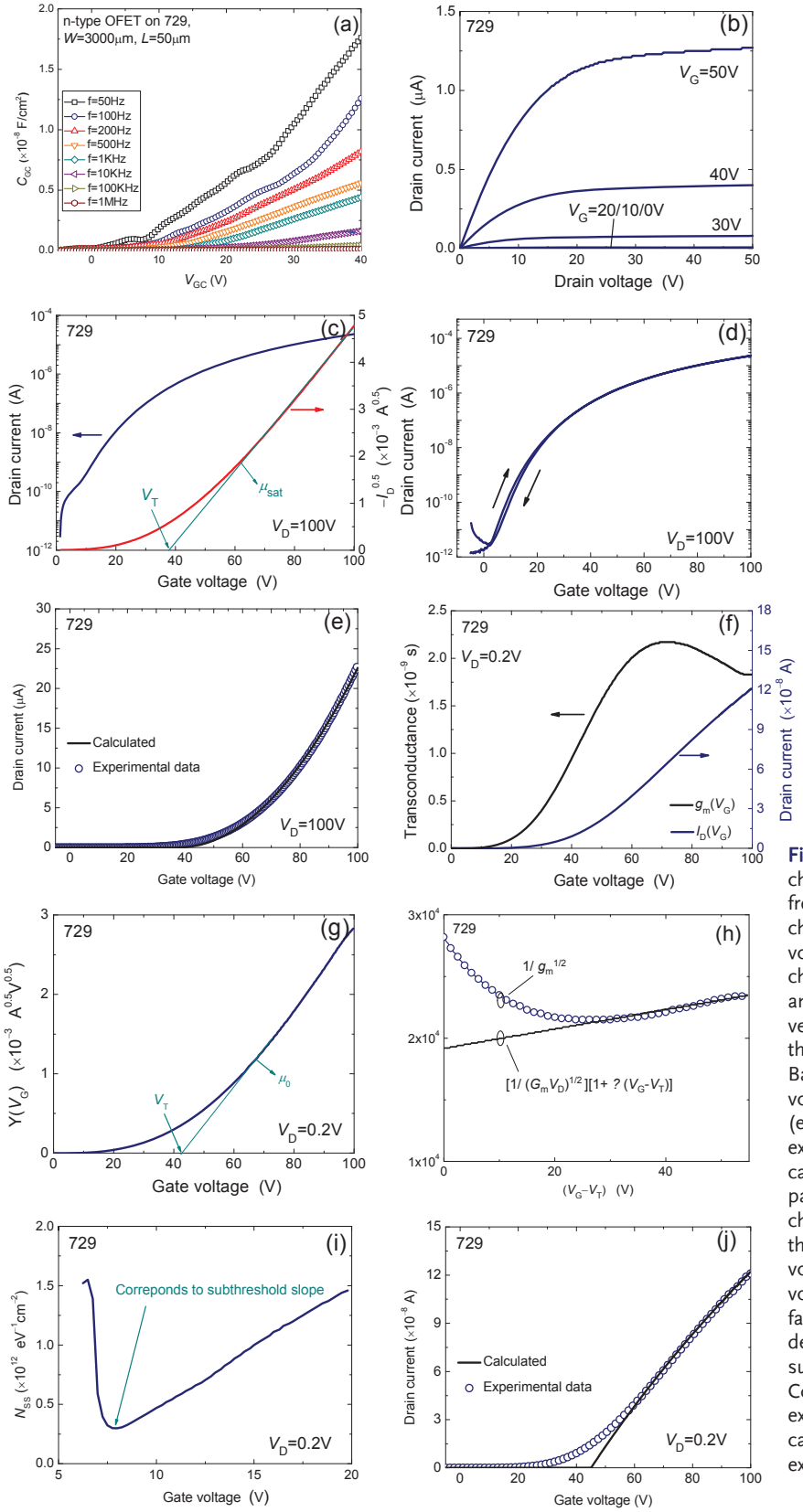


Figure 3.43 | (a) C-V characteristics measured at various frequencies. (b) Output characteristics at various gate voltages. (c) Transfer characteristics in saturation regime and the square root of drain current versus gate voltage for mobility and threshold voltage extractions. (d) Back and forth sweeping the gate voltage for hysteresis observation. (e) Comparison between the experimental data and the calculated ones by using extracted parameters. (f) Transfer characteristics in linear regime and the transconductance versus gate voltage. (g) Y function versus gate voltage. (h) Mobility attenuation factor evaluation. (i) Surface state density analysis by the subthreshold slope technique. (j) Comparison between the experimental data and the calculated ones by using the extracted parameters.

The high threshold voltage in these n-type OFETs is clearly not originated from the large charge injection barrier that is usually observed in n-type transistors and due to the energy difference between the contact metal work function and the OSC LUMO level. Because we didn't observe non-linear properties at small drain voltages, i.e. in linear operation and moreover, the contact resistance obtained by Y function method or by TLM is not very high compared to PTAA OFETs (727) that are fabricated with similar configurations and technologies.[11] Furthermore, the slow trap density and the surface states density are comparable to the PTAA counterparts. Therefore, such a much higher absolute value of threshold voltage might be due the fixed positive charge distributed in the gate dielectric, semiconductor film and at the dielectric/OSC interface which significantly shifts the flat band voltage to be positive and screens the gate electrical field, a much higher gate voltage is required to induce the same charge with respect to the PTAA OFETs.

3.10 STATIC CHARACTERIZATIONS OF TIPS-PENTACENE OFETS

The final set of samples we received from CEA-LITEN are TIPS-pentacene OFETs, the substrate code is 715. These OFETs exhibit remarkable high performance and good quality, all of the foregoing analyses show nearly ideal results in these transistors. For simplicity, we also select one transistor to illustrate results, T5(W=200μm, L=50μm). More results could be found in next chapter for the OFETs' I-V characteristics modeling and the carrier transport modeling.

First, C-V characteristics are shown in Fig. 3.44a. A plateau at high voltages is formed and it corresponds to C_i=0.8×10^{-9}F/cm^2 (f=100Hz). This value is much lower than the theoretical one C_{itheo}=1.48×10^{-9} F/cm^2. For further verification, we analyzed also the concurrently fabricated capacitor and the results are shown in Fig. 3.44b. The C-V curves converge at low frequencies and a constant plateau is formed, which gives C_i=1.58×10^{-9}F/cm^2, slightly higher than C_{itheo}=1.48×10^{-9} F/cm^2. This result indicates that such a theoretical C_{itheo} is applicable and thus is applied for next analysis. Meanwhile, the converging C-V data could be safely used for split C-V study and subsequently for effective mobility analysis.

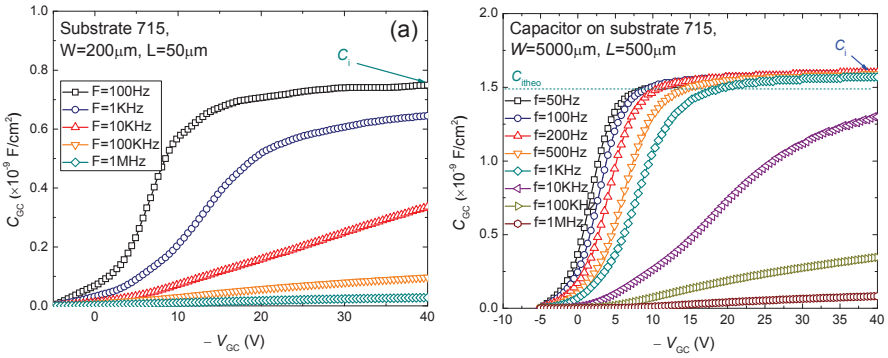


Figure 3.44 | C-V characteristics measured at various frequencies in a transistor (a) and in a

Next, we examined the output characteristics (cf. Fig. 3.45a), one can find good field-effect transistor behaviors and a good linearity at small drain voltages. And then, its transfer characteristics in saturation regime are analyzed (cf. Fig. 3.45b), the extracted V_T=−4.7V and μ_{sat}=2.5cm^2/Vs. The hysteresis is nearly unobservable; hence the relevant figure is not shown here. In linear regime (see Fig. 3.45c), the transfer characteristics curve exhibits a very good linearity over a large range of gate voltage and the transconductance reaches a maxima around V_G=−20V and afterwards decreases with V_G. The Y function is plotted versus gate voltage as seen in Fig. 3.45d. One can obtain a V_T=−9.5V and μ_0=2.67cm^2/Vs. In general, the parameters extracted in linear regime are preferred for analysis in order to avoid the effects of channel non-uniformity and the gate/drain voltage dependent mobility etc. The V_T=−9.5V by Y function is much higher than that V_T=−4.7V by classical method in this transistor, even though both extrac-

tions show good linearity. We will see in Table 3.2, Y function displays much greater stability from transistor-to-transistor, its good linearity actually reflects a precise charge threshold voltage. To know the contact resistance value, an evaluation of mobility attenuation factor is conducted, cf. Fig. 3.45e. A very good fitting is attained, thus we have θ=0.0022/V, R_{sd}=1.5×10^{5}Ω or W×R_{sd}=2.8×10^{3}Ωcm. This value is smaller than in PTAA OFETs on substrate 727 and it is the smallest contact resistance in all our studied printing OFETs. The surface state density is also analyzed by subthreshold slope, it is found that SS=6.6V/decade and N_{SS}=1×10^{12}/eVcm^2, cf. Fig. 3.45f. This value remains an average level with respect to those in PTAA OFETs (727) made by similar technology, as expected. Finally, we compare the experimental data and the calculated ones by using the extracted parameters. A good agreement is obtained in Fig. 3.45g, implying the validity of the applied Y function method. For further exploration of the contribution of mobility attenuation in these TIPS-pentacene OFETs, we checked several transistors having various channel lengths and widths and their θ are plotted versus the channel width normalized G_m. The slope of the linear regression indicates the channel width normalized contact resistance for this group of OFETs (here W×R_{sd}=3×10^{3}Ωcm), very close to the value directly obtained by Y function method in the example OFET T5 W×R_{sd}=2.8×10^{3}Ωcm. Moreover, the intercept in y-axis θ_0=7.7×10^{-4} 1/V is very small, i.e. the phonon scattering and surface roughness impact on mobility attenuation can be neglected and a direct calculation of R_{sd} by θ in individual transistor can be applied.

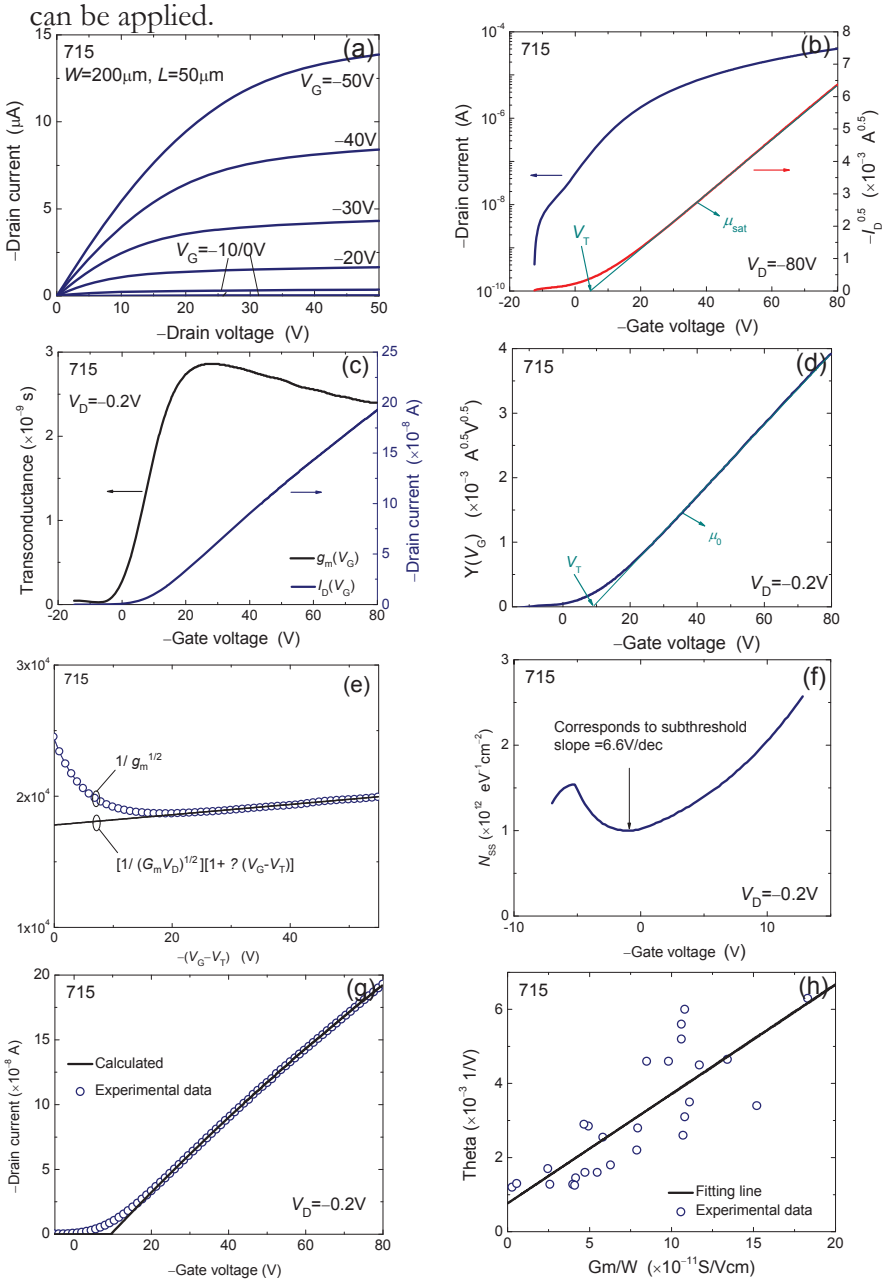


Figure 3.45 | (a) Output characteristics at various gate voltages. (b) Transfer characteristics in saturation regime and the square root of drain current versus gate voltage for mobility and threshold voltage extractions. (c) Transfer characteristics in linear regime and the transconductance versus gate voltage. (d) Y function versus gate voltage. (e) Mobility attenuation factor evaluation. (f) Surface state density analysis by subthreshold slope technique. (g) Comparison between the experimental data and the calculated ones by using the extracted parameters. (h) The mobility attenuation factor versus the transconductance parameter for several OFETs having different W and L.

■ Low-temperature measurements

We performed two rounds of low-temperature measurements on this set of TIPS-pentacene OFETs. On the first round, the temperature was decreased to liquid nitrogen temperature, i.e. 77K. On another round, the temperature was down to liquid helium temperature, namely 4.3K but the actually minimum temperature was 15K due to the large chamber of cryo-station. Because many results of the second round will be discussed in the next chapter, here we only focus on the first test of the lowest T=77K. For the sake of scaling analysis, we selected 10 OFETs with 6 channel lengths. Hence, the M-TLM can be applied at each temperature for the gate-voltage dependent contact resistance extraction. As usual, one transistor T5(W=200μm, L=50μm) is chosen for results illustration.

■■ *C-V characteristics in capacitor*

Owing to the large dispersion in OFETs' C-V characteristics, here we just analyze on a Metal-Insulator-Semiconductor (MIS) capacitance. Its C-V characteristics measured at a low f=50Hz and at various temperatures are shown in Fig. 3.46. One can see that the height of plateau slightly decreases with temperature and at the same time, the C-V curves move to higher (absolute) gate bias at low temperatures. The explanation for the former is not clear but the latter is due to the increased absolute value of flat-band voltage. Relatively more charge carriers (holes here) are trapped at low temperatures; they screen the gate field and raise the threshold voltage. This result will be confirmed by the threshold voltage shift with temperature.

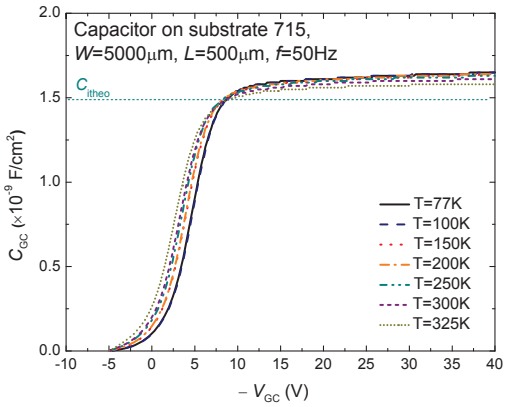


Figure 3.46 | C-V characteristics of a capacitor measured at various temperatures and f=50Hz.

■■ *I-V characteristics*

The transfer characteristics in saturation regime at low temperature are not stable, in principal with a non-linearity in the plot of the square root of drain current versus gate voltage. At higher temperature, such a non-linearity is less pronounced, see Fig. 3.47a. Hence, the mobility and the threshold voltage extracted by those curves are not reliable. However, we can see that the Y functions in Fig. 3.47b, corresponding to the transfer characteristics in linear regime, are always very linear, implying a greater accuracy. Therefore, the low-field mobility and the threshold voltage extracted by Y function are used for detailed temperature dependent investigation.

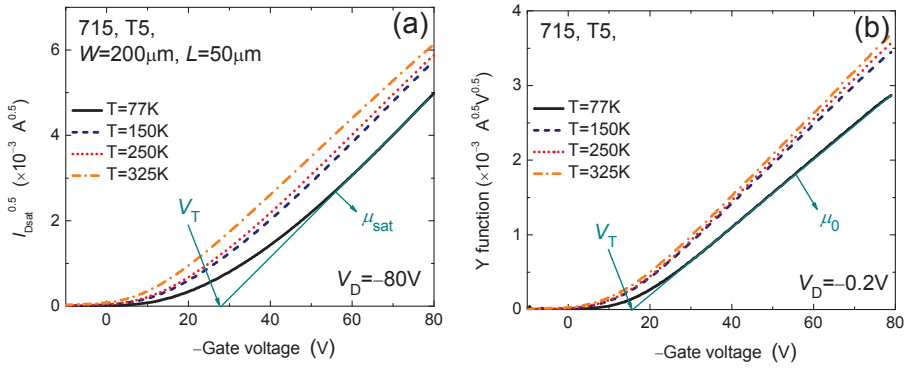


Figure 3.47 | (a) The square root of drain current in saturation regime versus gate voltage at various temperatures. (b) Y function versus gate voltage at various temperatures.

Mobility versus T

The mobility of all studied OFETs exhibits a thermal activation property, as shown in Fig. 3.48a for the example OFET T5. From this figure, one can see that the low-field mobility increases monotonically with temperature, from 2 cm^2/Vs to 2.6 cm^2/Vs as the temperature varies from 77K to 325K. Actually, if applying lower temperature, we can observe a nearly constant mobility at low temperatures, this result will be discussed in the next chapter. The mobility is plotted in Arrhenius plot (cf. Fig. 3.48b), and the data points are well located in the fitting straight line. However, the related activation energy E_a in the conventional thermally activated hopping transport expressed as $\mu_0=\mu_{00}\exp(-E_a/kT)$ is very small, here $E_a\approx3$meV with μ_{00} being a specific mobility and k being the Boltzmann constant. Such a so small E_a and non-zero mobility at low T clearly cannot justify the fully hopping transport. More details on transport modeling could be also found in next chapter.

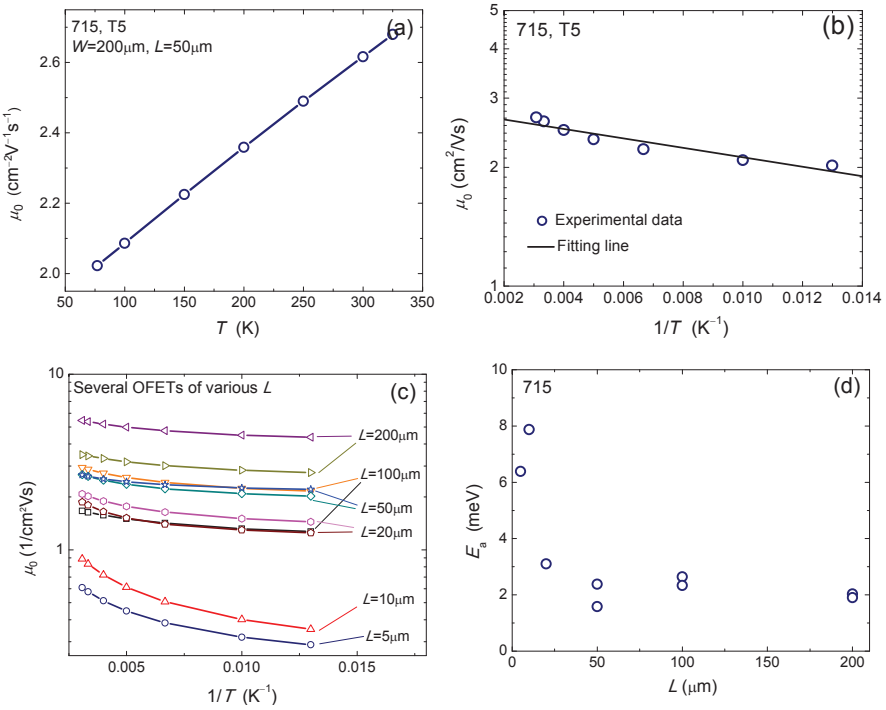


Figure 3.48 | (a) Low-field mobility in an OFET at various temperatures. (b) Arrhenius plot of mobility in this OFET. (c) Arrhenius plot of mobility for various OFETs having different channel length. (d) Activation energy of low-field mobility versus channel length.

The mobility in all studied OFETs are plotted in Fig. 3.48c, and one can find that two short-channel OFETs show much smaller mobility and stronger temperature dependence. This might be due to the contact effect in BC OFETs. Indeed, during the fabrication of OSC film (by vacuum evaporation or printing), the self organization of organic material is disrupted by the presence of pre-patterned metal contacts. Hence very small grains are formed in the vicinity of contacts and a large number of traps reside in this region. The carrier transport in this region is more accomplished by hopping, leading to lower mobility and higher activation energy with respect to that in channel where the relative hopping contribution to overall carrier transport is less pronounced. Thus we plot the activation energy of this mobility versus channel length, as shown in Fig. 3.48d. It's clear that E_a decreases with L and stabilizes in longer-channel devices, confirming the contact impact on mobility. Similar result is discussed later but the E_a values are a little different. This is because there the selected data are all at higher temperatures where the mobility exhibits obvious thermal activation behavior, thus the obtained E_a is higher than the results shown here. In any case, the temperature dependent tendency is not changed.

Threshold voltage versus T

The threshold voltage is obviously shifted to smaller(less negative values) while temperature is increasing, as seen in Fig. 3.49a. This shift in threshold voltage with temperature has been discussed in ref.[50] and was attributed to the shallow traps, according to the equation below:

$$\Delta Q_T = \Delta V_T C_i \tag{3.56}$$

where ΔQ_T is the trapped charge per unit surface. Here ΔV_T=1.34V (77K to 325K) corresponds to ΔQ_T=2×10^{-9} C/cm^2. At lower temperatures, the trapped charge cannot be thermally released. These equivalently fixed holes shift the flat-band voltage to be more negative and at the same time screen the gate field, thus raising the threshold voltage. Fig. 3.49b shows the threshold voltage versus temperature in all OFETs. One can find that they all show similar temperature dependences except for the shortest-channel OFET (R14, L=5μm) in which deep traps may reside in, thus the charge trapping is different from that by shallow traps.

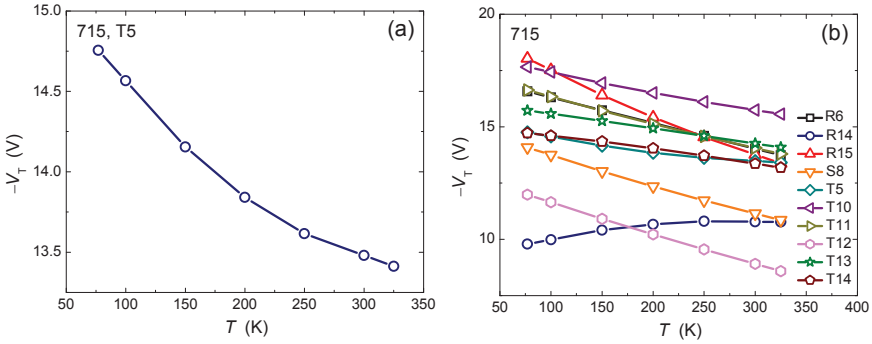


Figure 3.49 | (a) Threshold voltage versus temperature in an OFET T5. (b) The same figure as (a) for several OFETs having various channel lengths.

■■■ *Contact resistance versus T*

We observed a decrease of contact resistance with temperature, as seen in Fig. 3.50. It might be due to the related carrier transport in the contact region, analogous to the thermally enhanced mobility in the channel. As discussed above, a large number of traps distribute in the contact region and the carrier transport is more via thermally activated hopping. Heating certainly increases the hopping rate and thus the contact conductivity, manifesting a decreased contact resistance with temperature.

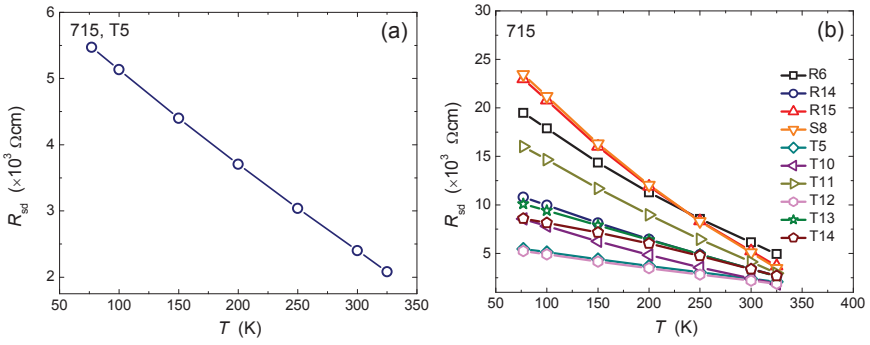


Figure 3.50 | (a) Contact resistance versus temperature in an OFET T5. (b) The same figure as (a) for several OFETs having various channel lengths.

Note that the contact resistances studied above are extracted by Y function method and they are assumed to be constant with respect to the gate voltage. Thanks to a set of OFETs having various channel lengths, we could perform the transfer-line method (TLM) for a gate-voltage dependent contact resistance extraction and thus, observe their evolution with temperature. During TLM analysis, we found that the linear regression is poor at lower temperature, especially in the conventional TLM (C-TLM). This is because in C-TLM the linear variation versus channel length is controlled by the channel resistance contribution. At low temperature, the dispersion of mobility and threshold voltage is very large due to the random charge trapping from transistor-to-transistor. At higher temperatures, the trapped charges are gradually released and the channel resistance exhibits better scaling. On the other hand, in M-

TLM analysis this effect is less significant because the linear variation against $1/L$ in M-TLM is mainly governed by the contact resistance contribution. Even though charge trapping plays a similar role in affecting the contact transport as on the channel one, however the dispersion of mobility and threshold voltage is absent for contact resistance and thereby, the contact resistance exhibits better uniformity at low temperature. That's why a better fitting is observed in M-TLM over C-TLM, as seen in Fig. 3.51. The extracted contact resistance by M-TLM is shown in Fig. 3.52a.

Many works reported that the Meyer-Neldel rule (MNR) is held for the contact conductance (G_C).[16] MNR model describes the charge transport through exponential density of states (DOS) and it is an empirical law and has been mostly observed in transport in disordered media, although the origin of the MNR is still unclear. Here,

$$G_C = \frac{I_D}{V_C} = \frac{1}{R_{sd}} \tag{3.57}$$

where V_C is the potential drop at the contact. For the contact conductance, MNR can be written as:

$$G_C = G_{C,0} \exp\left(-\frac{E_a}{kT}\right) \tag{3.58}$$

where k is the Boltzmann constant and T is the absolute temperature. The exponential prefactor ($G_{C,0}$) is exponentially correlated with the activation energy E_a via

$$G_{C,0} = G_{C,00} \exp\left(\frac{E_a}{E_{MN}}\right) \tag{3.59}$$

where E_{MN} is the so-called Meyer-Neldel energy which is thought to give the width of DOS. MNR-governed conduction has been reported in the channel of organic thin-film transistors. In these reports, the MNR originated from multiple trapping transports through exponential DOS.

Basing on this model, the Arrhenius plots of G_C at each gate voltage are shown in Figs. 3.52b,c. From the latter figure, one can find that no crossing point is formed for this group of fitting lines at various V_G since the change of activation energy with V_G is very slight, in particular at high V_G. Therefore, the MNR model is not valid in our case, implying the fairly good quality (low trap density and not exponentially distributed traps DOS) poly-crystalline organic film here, the carrier transport in contact region is different from that in amorphous media.

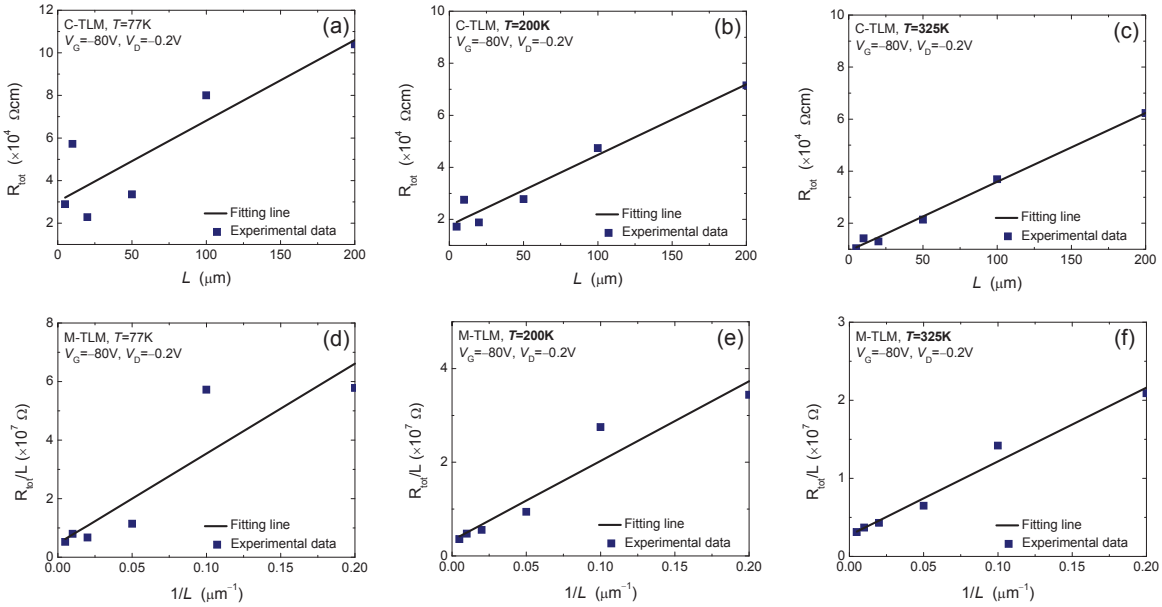


Figure 3.51 | (a-c) Conventional TLM for contact resistance evaluation at various temperatures. (d-f) Modified TLM for the same extractions as shown in (a-c).

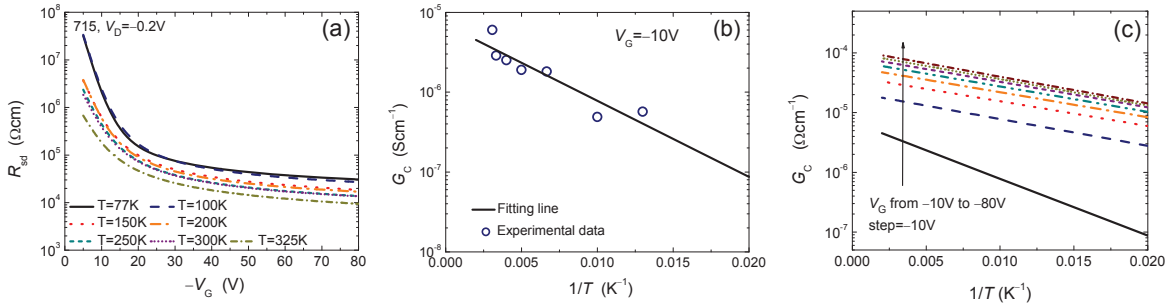


Figure 3.52 | (a) Contact resistance evaluated by M-TLM at various temperatures. (b) Arrhenius plot of contact conductance at V_G=–10V. (c) same plot as (b) but at various gate voltages.

■■■ *Subthreshold slope versus T*

The subthreshold slope is also clearly dependent on the temperature, as seen in Fig. 3.53. This is because its value is proportional to *kT* and thus increases with temperature. The influence of traps has a tendency more likely to reduce the diminution of *SS* at low temperature due to their augmentation of band edge.

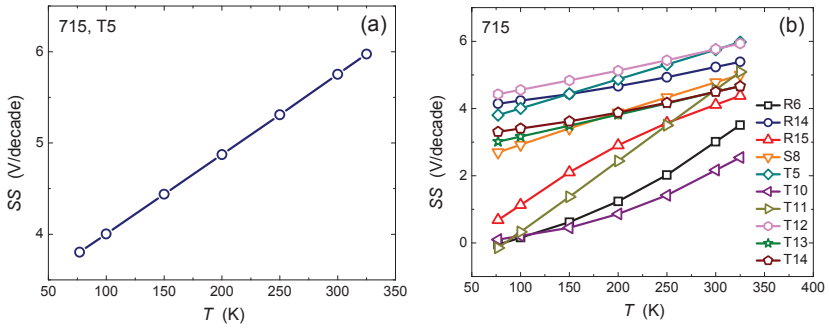


Figure 3.53 | (a) Subthreshold slope versus temperature extracted in linear regime and in an OFET T5. (b) The same figure as (a) for several OFETs having various channel lengths.

From Fig. 3.53b, one may find very small *SS* at low temperature. For example, the black square curve for OFET R6, the transfer characteristics at various *T* in semi-log scale are shown in Figs. 3.54a-c. At low temperature, the disappeared data points are due to the negative drain current values and they cannot be correctly displayed in log scale. Hence, their *SS* extraction becomes difficult. Larger surface state density is obtained at higher temperature, as seen in Figs. 3.54d-f. At low temperature, one can find less diminution of *SS* due to the effect of traps which compensates the temperature dependence of the *SS*.

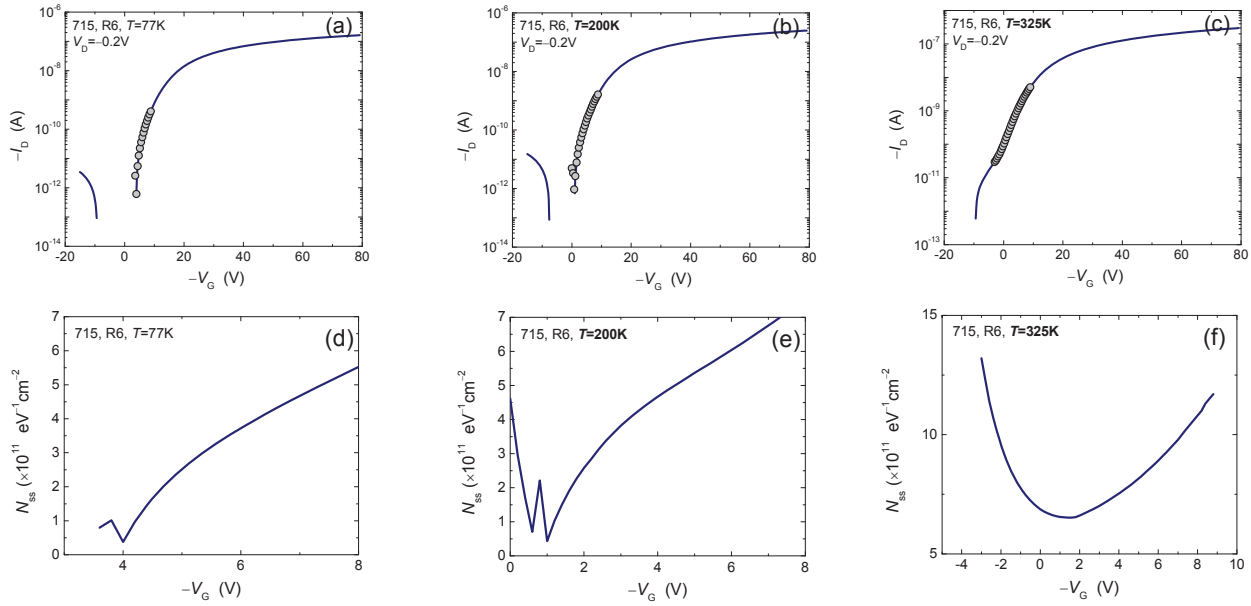


Figure 3.54 | (a-c) Extraction of subthreshold slope in an OFET R6 at various temperatures. (e-f) Corresponding surface state density analysis at various temperatures.

3.11 CONCLUSION

A detailed description of OFETs' electrical characterizations has been presented. We first discussed the mostly used method in the community for the mobility and threshold voltage extraction by the transfer characteristics in saturation regime. It was found not very reliable and not powerful enough (e.g. for contact resistance extraction). And then we introduced the Y function method and it was proved to be a powerful method, with high reliability and accuracy. Afterwards, one addressed other methods for the principal parameters extraction, including also our modified and power TLM. In the end, we briefly presented the results of our studied OFETs in this thesis; some of extracted parameters are attached at the end of this chapter.

TABLE 3.2 Summary of the parameters extracted by DC data in some of studied OFETs

Transistor					Conventional method (saturation regime)			Y function method (linear regime)				
OSC	code	W (μm)	L (μm)	C_i (F/cm^2)	μ_{sat} (cm^2/Vs)	V_T (V)	I_{on}/I_{off}	μ (cm^2/Vs)	V_T (V)	I_{on}/I_{off}	R_{sd} (Ωcm)	SS (V/dec)
Pentacene-RIKEN	TC1	500	150	7.5×10^{-8}	0.22	1.3	2.2×10^{7}	0.43	−2.1	3.5×10^{6}	2800	0.86
Pentacene-RIKEN	TC2	500	100	9.3×10^{-8}	0.17	1.3	2.5×10^{7}	0.34	−1.6	3.4×10^{7}	3100	0.99
Pentacene-RIKEN	TC3	500	50	9.5×10^{-8}	0.2	2.4	1.8×10^{4}	0.36	0.7	5×10^{3}	3400	0.39
Pentacene-RIKEN	BC1	500	150	4.9×10^{-8}	0.07	1.9	2.2×10^{6}	0.12	0.7	2.7×10^{6}	5.6×10^{4}	0.06
Pentacene-RIKEN	BC2	500	100	4.7×10^{-8}	0.06	3.1	6.1×10^{3}	0.07	2.3	1.5×10^{3}	1.1×10^{5}	0.43
Pentacene-RIKEN	BC3	500	50	4.5×10^{-8}	0.03	1.8	2.9×10^{6}	0.04	0.8	1×10^{7}	1.6×10^{5}	0.3
Pentacene-NIMS	50nm	1000	60	8×10^{-8}(t)	0.13	1.1	8.2×10^{3}	0.16	0.03	2.6×10^{3}	NA	1.3
Pentacene-NIMS	50nm	1000	80	1.8×10^{-7}	0.14	0.7	1.3×10^{4}	0.15	−0.3	3.2×10^{3}	NA	1.3
Pentacene-NIMS	50nm	1000	100	1.4×10^{-7}	0.15	0.7	1.3×10^{4}	0.17	−0.25	3×10^{3}	NA	1.4
Pentacene-NIMS	50nm	1000	120	8×10^{-8}(t)	0.18	0.8	1×10^{4}	0.2	−0.18	2.2×10^{3}	NA	1.3
Pentacene-NIMS	100nm	1000	60	2.4×10^{-7}	0.06	−0.4	1.6×10^{5}	0.07	−1	2.5×10^{4}	NA	1
Pentacene-NIMS	100nm	1000	80	2×10^{-7}	0.08	−0.3	4×10^{5}	0.1	−0.9	1×10^{5}	NA	1
Pentacene-NIMS	100nm	1000	100	8×10^{-8}(t)	0.08	3.1	5.7×10^{4}	0.1	0.06	2.3×10^{3}	NA	1.3
Pentacene-NIMS	100nm	1000	120	1.5×10^{-7}	0.09	−0.9	7.7×10^{4}	0.09	−1.3	1×10^{4}	NA	1.1
PTAA-IZM	30-D8	6×10^{4}	30	1.3×10^{-9}	2.1×10^{-4}	−6.5	NA	6.6×10^{-4}	−16.7	2.2×10^{3}	1.1×10^{7}	0.6
PTAA-IZM	20-D4	4×10^{4}	20	1.5×10^{-9}	1.9×10^{-4}	−2.4	NA	7.1×10^{-4}	−14	140	4×10^{6}	10
PTAA-IZM	16-D3	3.2×10^{4}	16	1.4×10^{-9}	0.9×10^{-4}	−1.3	NA	5.4×10^{-4}	−18	305	7.5×10^{6}	0.2
PTAA-LITEN	379-l2c1	500	50	2.4×10^{-8}	1.5×10^{-3}	−13.2	4.1×10^{4}	0.9×10^{-3}	−9.2	6.9×10^{3}	5.4×10^{6}	1.5
PTAA-LITEN	379-l3c4	1000	50	3.6×10^{-8}	0.7×10^{-3}	−10.3	7.9×10^{4}	0.7×10^{-3}	−9	1.2×10^{4}	4.7×10^{6}	1.7
PTAA-LITEN	379-l5c5	1000	80	1.9×10^{-8}	3.1×10^{-3}	−12.6	1.7×10^{5}	1.9×10^{-3}	−9	2.2×10^{3}	4.4×10^{6}	0.2
PTAA-LITEN	379-l3c2	1000	80	1.8×10^{-8}	2.1×10^{-3}	−10.6	1.2×10^{5}	1.6×10^{-3}	−8.8	1.9×10^{4}	3.7×10^{6}	1.6
PTAA-LITEN	379-l3c3	1000	100	1.6×10^{-8}	3.4×10^{-3}	−9.8	1.6×10^{5}	2.8×10^{-3}	−11	4.5×10^{4}	4.1×10^{6}	0.07
PTAA-LITEN	379-l4c6	2000	100	1.2×10^{-8}	3.7×10^{-3}	−12.3	6.3×10^{4}	3.7×10^{-3}	−8.3	3.5×10^{3}	4.5×10^{6}	0.12
PTAA-LITEN	404-l4c1	500	50	2.7×10^{-8}	4.2×10^{-3}	−17.2	4.4×10^{4}	0.9×10^{-3}	−19.7	6.6×10^{4}	2.8×10^{6}	1.86
PTAA-LITEN	404-l1c5	1000	50	1.8×10^{-8}	5.2×10^{-3}	−17.6	4.6×10^{7}	1.8×10^{-3}	−19.3	5.1×10^{5}	4.1×10^{6}	1.84
PTAA-LITEN	404-l2c3	2000	50	1.6×10^{-8}	6×10^{-3}	−14	2.2×10^{6}	2.4×10^{-3}	−15	1.5×10^{5}	2.9×10^{6}	1.68
PTAA-LITEN	404-l1c2	1000	80	1.1×10^{-8}	7.9×10^{-3}	−13.8	5.1×10^{7}	3.8×10^{-3}	−17	6.6×10^{4}	4.8×10^{6}	1.86
PTAA-LITEN	404-l3c3	1000	100	0.9×10^{-8}	9.3×10^{-3}	−17.8	4.5×10^{5}	1.3×10^{-3}	−19.5	1×10^{5}	7.6×10^{6}	1.12
PTAA-LITEN	404-l2c4	2000	100	0.8×10^{-8}	12×10^{-3}	−13.8	6.4×10^{5}	5.7×10^{-3}	−14.3	1.8×10^{5}	3.4×10^{6}	1.39
PTAA-LITEN	727-R14	2000	5	1.48×10^{-9}(t)	0.012	−9.3	1.2×10^{5}	0.01	−8.5	2.1×10^{3}	1.9×10^{5}	2.45
PTAA-LITEN	727-R15	2000	10	1.48×10^{-9}(t)	0.022	−8.5	5.2×10^{4}	0.016	−8.1	1.5×10^{3}	2×10^{5}	2.42
PTAA-LITEN	727-T14	600	20	1.48×10^{-9}(t)	0.03	−10.5	3×10^{6}	0.026	−9.4	6.4×10^{3}	1.5×10^{5}	1.65
PTAA-LITEN	727-S13	2000	50	1.48×10^{-9}(t)	0.035	−8.6	2×10^{5}	0.034	−7.5	1.4×10^{3}	2.2×10^{5}	0.21
PTAA-LITEN	727-R6	1000	100	1.48×10^{-9}(t)	0.031	−7	8.6×10^{4}	0.033	−7.2	1.3×10^{3}	2.6×10^{5}	0.48
PTAA-LITEN	727-T13	1000	50	1.48×10^{-9}(t)	0.033	−10.5	1.9×10^{5}	0.035	−9.1	7.3×10^{3}	1.2×10^{5}	0.22
N1400	729-A3	10000	20	1.48×10^{-9}(t)	0.02	16.6	1.6×10^{4}	0.02	14.8	3.7×10^{3}	NA	3.3
N1400	729-B14	200	50	1.48×10^{-9}(t)	0.3	32.3	2.2×10^{4}	0.35	39	6.3×10^{3}	1.8×10^{4}	0.37
N1400	729-C7	5000	100	1.48×10^{-9}(t)	0.19	30.4	1.4×10^{4}	0.28	41	6.4×10^{4}	NA	0.5
N1400	729-D13	1000	20	1.48×10^{-9}(t)	0.07	27.7	1.1×10^{4}	0.12	40	1.3×10^{5}	5.9×10^{4}	0.18
N1400	729-E13	1000	50	1.48×10^{-9}(t)	0.22	31.7	2×10^{4}	0.25	40.5	8.5×10^{3}	5.9×10^{4}	0.4

N1400	729-E14	600	20	1.48×10^{-9}(t)	0.1	27.7	1.1×10^{4}	0.15	37.5	1.7×10^{5}	5.9×10^{4}	0.47
TIPS-pentacene	715-T4	2000	100	1.48×10^{-9}(t)	2.71	–12.2	5.6×10^{5}	2.8	–15	1.6×10^{4}	3.5×10^{3}	4.7
TIPS-pentacene	715-T5	200	50	1.48×10^{-9}(t)	2.45	–4.7	7.4×10^{3}	2.7	–9.5	1.1×10^{3}	2.8×10^{3}	6.5
TIPS-pentacene	715-T11	2000	200	1.48×10^{-9}(t)	3.34	–10.4	1.7×10^{5}	3.5	–13.3	4.3×10^{3}	5×10^{3}	4.8
TIPS-pentacene	715-T14	600	20	1.48×10^{-9}(t)	1.33	–11.6	1.4×10^{5}	1.8	–12.2	2.9×10^{3}	3.5×10^{3}	4.9
TIPS-pentacene	715-R14	2000	5	1.48×10^{-9}(t)	0.13	10	7.8×10^{2}	0.6	–0.6	1.3×10^{4}	3.4×10^{3}	5.5
TIPS-pentacene	715-R15	2000	10	1.48×10^{-9}(t)	0.21	–8.4	6.5×10^{3}	0.8	–10.8	2.6×10^{4}	3.9×10^{3}	4.8

For C_i, "t" represents the value calculated from the technological dielectric thickness and theoretical permittivity.

TABLE 3.3 Summary of the parameters in TIPS-pentacene OFETs at low temperature (round 1, down to 77K)

Transistor					Conventional method (saturation regime)			Y function method (linear regime)				
Code	Temperature	W (μm)	L (μm)	C_i (F/cm²)	μ_{sat} (cm²/Vs)	V_T (V)	I_{on}/I_{off}	μ (cm²/Vs)	V_T (V)	I_{on}/I_{off}	R_{sd} (Ωcm)	SS (V/dec)
715-R14	77K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.28	–8.1	5.9×10^{2}	1.2×10^{4}	4.4
715-R14	100K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.32	–11.3	3.9×10^{3}	9.5×10^{3}	4.1
715-R14	150K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.4	–11.2	3.7×10^{3}	7×10^{3}	4.2
715-R14	200K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.44	–10.9	2.7×10^{3}	6.1×10^{3}	4.5
715-R14	250K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.51	–11.2	2.3×10^{3}	4.7×10^{3}	4.8
715-R14	300K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.57	–11.8	2.1×10^{3}	3.6×10^{3}	5.2
715-R14	325K	2000	5	1.48×10^{-9}(t)	NA	NA	NA	0.62	–9.6	1×10^{3}	2.6×10^{3}	5.5
715-R15	77K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.28	–8.1	5.9×10^{2}	1.2×10^{4}	4.4
715-R15	100K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.32	–11.3	3.9×10^{3}	9.5×10^{3}	4.1
715-R15	150K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.4	–11.2	3.7×10^{3}	7×10^{3}	4.2
715-R15	200K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.44	–10.9	2.7×10^{3}	6.1×10^{3}	4.5
715-R15	250K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.51	–11.2	2.3×10^{3}	4.7×10^{3}	4.8
715-R15	300K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.57	–11.8	2.1×10^{3}	3.6×10^{3}	5.2
715-R15	325K	2000	10	1.48×10^{-9}(t)	NA	NA	NA	0.62	–9.6	1×10^{3}	2.6×10^{3}	5.5
715-T12	77K	200	20	1.48×10^{-9}(t)	1.72	–19.9	1.44×10^{5}	1.36	–12.8	2.8×10^{3}	6×10^{3}	4.28
715-T12	100K	200	20	1.48×10^{-9}(t)	1.93	–18.1	5.8×10^{4}	1.55	–11.2	1.5×10^{3}	4.5×10^{3}	4.67
715-T12	150K	200	20	1.48×10^{-9}(t)	2.02	–16.6	3.5×10^{4}	1.7	–10.3	1.2×10^{3}	3.6×10^{3}	4.92
715-T12	200K	200	20	1.48×10^{-9}(t)	2.05	–15.8	2.8×10^{4}	1.79	–10	1.1×10^{3}	3.3×10^{3}	5.07
715-T12	250K	200	20	1.48×10^{-9}(t)	2.07	–15.1	2.4×10^{4}	1.85	–9.95	1.1×10^{3}	3.1×10^{3}	5.18
715-T12	300K	200	20	1.48×10^{-9}(t)	2.1	–12.9	1.4×10^{4}	2	–9.23	9.3×10^{2}	2.4×10^{3}	5.52
715-T12	325K	200	20	1.48×10^{-9}(t)	1.93	–8.5	5.6×10^{3}	2.12	–8.1	9.6×10^{2}	1.6×10^{3}	6.31
715-T14	77K	600	20	1.48×10^{-9}(t)	1.68	–21.4	5.75×10^{5}	1.35	–14.4	2.6×10^{4}	7.5×10^{3}	3.45
715-T14	100K	600	20	1.48×10^{-9}(t)	1.65	–21.5	6.77×10^{5}	1.26	–14.6	3.2×10^{4}	8.4×10^{3}	3.42
715-T14	150K	600	20	1.48×10^{-9}(t)	1.6	–21.9	9.75×10^{5}	1.26	–15	4.6×10^{4}	9.1×10^{3}	3.3
715-T14	200K	600	20	1.48×10^{-9}(t)	1.76	–19.5	2.82×10^{5}	1.54	–13.8	1.2×10^{4}	5.5×10^{3}	3.92
715-T14	250K	600	20	1.48×10^{-9}(t)	1.75	–19.1	2.52×10^{5}	1.56	–13.7	1.2×10^{4}	5.4×10^{3}	3.9
715-T14	300K	600	20	1.48×10^{-9}(t)	1.81	–17	1.6×10^{5}	1.77	–13.7	7.5×10^{3}	3.5×10^{3}	4.33
715-T14	325K	600	20	1.48×10^{-9}(t)	1.53	–13	7.49×10^{4}	1.93	–13	4.1×10^{3}	2.5×10^{3}	4.92
715-T5	77K	200	50	1.48×10^{-9}(t)	2.44	–21.5	8.6×10^{5}	1.79	–16.1	2.8×10^{5}	6.2×10^{3}	3.49
715-T5	100K	200	50	1.48×10^{-9}(t)	2.78	–18.2	1.6×10^{5}	2.23	–13.7	1.2×10^{4}	4.6×10^{3}	4.23
715-T5	150K	200	50	1.48×10^{-9}(t)	2.86	–17.1	1×10^{5}	2.36	–13.1	6.5×10^{3}	4×10^{3}	4.64
715-T5	200K	200	50	1.48×10^{-9}(t)	2.86	–16.4	1×10^{5}	2.49	–13.6	7.4×10^{3}	3.5×10^{3}	4.82
715-T5	250K	200	50	1.48×10^{-9}(t)	2.87	–15.6	7.9×10^{4}	2.53	–13.3	5.3×10^{3}	3.2×10^{3}	5.1
715-T5	300K	200	50	1.48×10^{-9}(t)	2.85	–14.8	9.1×10^{4}	2.63	–14.6	8×10^{3}	2.6×10^{3}	5.58
715-T5	325K	200	50	1.48×10^{-9}(t)	2.69	–10.6	2.2×10^{4}	2.62	–12.6	2.5×10^{3}	1.8×10^{3}	6.26
715-T13	77K	1000	50	1.48×10^{-9}(t)	2.72	–20.1	9.4×10^{5}	2.23	–15.6	2.6×10^{6}	9.9×10^{3}	2.87
715-T13	100K	1000	50	1.48×10^{-9}(t)	2.85	–20.4	8×10^{5}	2.2	–15.7	6.3×10^{4}	1×10^{4}	3.28
715-T13	150K	1000	50	1.48×10^{-9}(t)	2.89	–18.9	4.2×10^{5}	2.39	–15.2	2.9×10^{4}	7.1×10^{3}	3.58
715-T13	200K	1000	50	1.48×10^{-9}(t)	2.88	–18.2	3.2×10^{5}	2.44	–15	2×10^{4}	6.4×10^{3}	3.78
715-T13	250K	1000	50	1.48×10^{-9}(t)	2.84	–17	2×10^{5}	2.51	–14.5	1.2×10^{4}	5.3×10^{3}	4.01

715-T13	300K	1000	50	1.48×10^{-9}(t)	2.78	−15.3	1.5×10^{5}	2.63	−14.6	1.1×10^{4}	3.6×10^{3}	4.28
715-T13	325K	1000	50	1.48×10^{-9}(t)	2.45	−11.7	6.1×10^{4}	2.68	13.8	5.2×10^{3}	2.2×10^{3}	4.95
715-R6	77K	1000	100	1.48×10^{-9}(t)	1.53	−20.9	2.1×10^{7}	1.12	−17.2	2.7×10^{5}	2.43×10^{4}	0.3
715-R6	100K	1000	100	1.48×10^{-9}(t)	1.71	−18	7.6×10^{6}	1.39	−15.9	3.6×10^{4}	1.57×10^{4}	0.2
715-R6	150K	1000	100	1.48×10^{-9}(t)	1.73	−15.2	3.7×10^{7}	1.56	−15.2	4.4×10^{4}	9.56×10^{3}	0.29
715-R6	200K	1000	100	1.48×10^{-9}(t)	1.73	−15.7	3.2×10^{7}	1.54	−15.3	3.9×10^{4}	1.06×10^{4}	0.34
715-R6	250K	1000	100	1.48×10^{-9}(t)	1.71	−14.4	4.8×10^{6}	1.59	−14.9	6.2×10^{4}	8.94×10^{3}	0.25
715-R6	300K	1000	100	1.48×10^{-9}(t)	1.68	−13.1	2.1×10^{6}	1.64	−14.6	2.8×10^{5}	6.21×10^{3}	3.43
715-R6	325K	1000	100	1.48×10^{-9}(t)	1.64	−11.4	1.5×10^{5}	1.65	−13	1.2×10^{4}	4.53×10^{3}	4.3
715-S8	77K	1000	100	1.48×10^{-9}(t)	3.18	−20.8	2.4×10^{6}	2.03	−14.7	4.6×10^{6}	2.85×10^{4}	2.32
715-S8	100K	1000	100	1.48×10^{-9}(t)	3.37	−18.6	6.3×10^{5}	2.29	−13.5	3.1×10^{4}	1.93×10^{4}	3.13
715-S8	150K	1000	100	1.48×10^{-9}(t)	3.39	−15.8	1.8×10^{5}	2.55	−12.4	8×10^{3}	1.13×10^{4}	3.74
715-S8	200K	1000	100	1.48×10^{-9}(t)	3.35	−14.7	1.4×10^{5}	2.63	−12.1	6.3×10^{3}	9.28×10^{3}	3.91
715-S8	250K	1000	100	1.48×10^{-9}(t)	3.27	−13.2	8.2×10^{4}	2.74	−11.8	4.210^{3}	7.67×10^{3}	4.22
715-S8	300K	1000	100	1.48×10^{-9}(t)	3.17	−11.5	5.6×10^{4}	2.85	−11.4	3.1×10^{3}	5.6×10^{3}	4.56
715-S8	325K	1000	100	1.48×10^{-9}(t)	2.95	−8.5	2.2×10^{4}	2.95	−10.6	1.7×10^{3}	3.7×10^{3}	5.27
715-T10	77K	500	200	1.48×10^{-9}(t)	4.96	−20.5	4.6×10^{6}	3.98	−18.5	12.6×10^{4}	1.1×10^{4}	0.28
715-T10	100K	500	200	1.48×10^{-9}(t)	5.43	−17.5	1.3×10^{6}	4.74	−16.9	2.2×10^{4}	6.3×10^{3}	0.24
715-T10	150K	500	200	1.48×10^{-9}(t)	5.52	−16.2	1.2×10^{6}	5.02	−16.3	3×10^{4}	4.6×10^{3}	0.25
715-T10	200K	500	200	1.48×10^{-9}(t)	5.53	−16.1	1×10^{6}	5.13	−16.4	3.3×10^{4}	4.5×10^{3}	0.38
715-T10	250K	500	200	1.48×10^{-9}(t)	5.55	−15.4	9.74×10^{5}	5.21	−16.2	4.4×10^{4}	3.6×10^{3}	0.13
715-T10	300K	500	200	1.48×10^{-9}(t)	5.52	−14.6	8.33×10^{5}	5.37	−16.2	9.5×10^{4}	2.8×10^{3}	0.3
715-T10	325K	500	200	1.48×10^{-9}(t)	5.42	−12.7	4.3×10^{5}	5.42	−15.1	1.7×10^{4}	1.5×10^{3}	5
715-T11	77K	2000	200	1.48×10^{-9}(t)	3.52	−10.2	5.1×10^{6}	2.56	−17.2	1.3×10^{4}	1.91×10^{4}	0.28
715-T11	100K	2000	200	1.48×10^{-9}(t)	3.67	−17.7	6.3×10^{6}	2.94	−16	3.7×10^{4}	1.29×10^{4}	0.3
715-T11	150K	2000	200	1.48×10^{-9}(t)	3.67	−16	1×10^{6}	3.15	−15.3	6.9×10^{4}	9.49×10^{3}	0.38
715-T11	200K	2000	200	1.48×10^{-9}(t)	3.63	−14.8	5.1×10^{5}	3.28	−14.9	1.3×10^{4}	7.85×10^{3}	3.22
715-T11	250K	2000	200	1.48×10^{-9}(t)	3.59	−14	3.1×10^{5}	3.35	−14.6	4.1×10^{4}	6.87×10^{3}	3.78
715-T11	300K	2000	200	1.48×10^{-9}(t)	3.5	−12.7	2.1×10^{5}	3.44	−14.4	1.5×10^{4}	4.73×10^{3}	4.22
715-T11	325K	2000	200	1.48×10^{-9}(t)	3.38	−11.3	9.9×10^{4}	3.43	−13.5	5.1×10^{3}	2.37×10^{3}	4.98

For C_i, "t" represents the value calculated from the technological dielectric thickness and theoretical permittivity. To ensure the successful full range of low temperature measurement of all transistors, we didn't perform transfer characteristics measurement in saturation regime on the shortest two transistors (R14 and R15). The subthreshold slope values in orange have difficulty in evaluation as discussed in the text.

TABLE 3.4 Summary of the parameters in TIPS-pentacene OFETs at low temperature (round 2, down to 15K)

Transistor					Conventional method (saturation regime)			Y function method (linear regime)				
Code	Temperature	W (μm)	L (μm)	C_i (F/cm²)	μ_{sat} (cm²/Vs)	V_T (V)	I_{on}/I_{off}	μ (cm²/Vs)	V_T (V)	I_{on}/I_{off}	R_{sd} (Ωcm)	SS (V/dec)
715-R14	15K	2000	5	1.48×10^{-9}(t)	0.37	−23.7	3.68×10^{4}	0.29	−10.3	9.9×10^{2}	6.42×10^{3}	4.32
715-R14	25K	2000	5	1.48×10^{-9}(t)	0.36	−24	4.17×10^{4}	0.275	−10.7	1.05×10^{3}	6.54×10^{3}	4.27
715-R14	35K	2000	5	1.48×10^{-9}(t)	0.4	−23.2	2.25×10^{4}	0.31	−9.4	8.93×10^{2}	6.05×10^{3}	4.48
715-R14	45K	2000	5	1.48×10^{-9}(t)	0.35	−24.5	5.03×10^{4}	0.26	−11.1	1.13×10^{3}	7.13×10^{3}	4.21
715-R14	55K	2000	5	1.48×10^{-9}(t)	0.36	−24.1	3.93×10^{4}	0.28	−10.6	9.6×10^{2}	6.81×10^{3}	4.36
715-R14	65K	2000	5	1.48×10^{-9}(t)	0.33	−24.4	5.11×10^{4}	0.257	−11.3	1.17×10^{3}	7.25×10^{3}	4.2
715-R14	75K	2000	5	1.48×10^{-9}(t)	0.36	−24	3.91×10^{4}	0.27	−10.7	1.03×10^{3}	6.72×10^{3}	4.3
715-R14	85K	2000	5	1.48×10^{-9}(t)	0.35	−23.4	2.54×10^{4}	0.28	−10.2	1.06×10^{3}	6.8×10^{3}	4.38
715-R14	100K	2000	5	1.48×10^{-9}(t)	0.33	−23.8	3.49×10^{4}	0.26	−10.9	9.9×10^{2}	7×10^{3}	4.33
715-R14	120K	2000	5	1.48×10^{-9}(t)	0.41	−22.6	1.38×10^{4}	0.32	−8.9	8.3×10^{2}	5.95×10^{3}	4.67
715-R14	140K	2000	5	1.48×10^{-9}(t)	0.38	−23.3	2.11×10^{4}	0.29	−9.9	1×10^{3}	6.4×10^{3}	4.42
715-R14	160K	2000	5	1.48×10^{-9}(t)	0.44	−21.9	8.96×10^{3}	0.35	−8.2	1×10^{3}	5.69×10^{3}	4.73
715-R14	180K	2000	5	1.48×10^{-9}(t)	0.42	−22.3	1.12×10^{4}	0.33	−8.6	9.54×10^{2}	6.02×10^{3}	4.71
715-R14	200K	2000	5	1.48×10^{-9}(t)	0.46	−21.3	6.43×10^{3}	0.32	−5.6	1.96×10^{3}	4.2×10^{3}	4.71
715-R14	220K	2000	5	1.48×10^{-9}(t)	0.49	−19.6	3.84×10^{3}	0.41	−7.1	1.34×10^{4}	4.6×10^{3}	4.72
715-R14	240K	2000	5	1.48×10^{-9}(t)	0.49	−19.2	3.28×10^{3}	0.42	−6.8	1.16×10^{4}	4.5×10^{3}	4.86
715-R14	260K	2000	5	1.48×10^{-9}(t)	0.49	−18.4	2.68×10^{3}	0.44	−6.7	9.88×10^{3}	4.3×10^{3}	4.99

715-R14	280K	2000	5	1.48×10^{-9}(t)	0.49	−17.9	2.32×10^{3}	0.45	−6.6	8.49×10^{3}	4.2×10^{3}	5.13
715-R14	300K	2000	5	1.48×10^{-9}(t)	0.49	−16.6	1.79×10^{3}	0.48	−6.6	6.89×10^{3}	4×10^{3}	5.31
715-R14	320K	2000	5	1.48×10^{-9}(t)	0.49	−15.7	1.48×10^{3}	0.49	−6.3	5.77×10^{3}	3.8×10^{3}	5.54
715-R14	340K	2000	5	1.48×10^{-9}(t)	0.46	−13.7	1.21×10^{3}	0.52	−6.5	4.73×10^{3}	3.5×10^{3}	5.81
715-R15	15K	2000	10	1.48×10^{-9}(t)	0.27	−23.4	1.33×10^{5}	0.42	−20.8	8.13×10^{4}	1.28×10^{4}	4.2
715-R15	25K	2000	10	1.48×10^{-9}(t)	0.25	−23.9	1.9×10^{5}	0.38	−21.9	3.13×10^{5}	1.13×10^{4}	4.1
715-R15	35K	2000	10	1.48×10^{-9}(t)	0.25	−23.8	1.63×10^{5}	0.39	−21.7	1.72×10^{5}	1.1×10^{4}	4.2
715-R15	45K	2000	10	1.48×10^{-9}(t)	0.2	−24.8	4.25×10^{5}	0.32	−23.5	2.98×10^{5}	1.33×10^{4}	3.9
715-R15	55K	2000	10	1.48×10^{-9}(t)	0.23	−24.3	2.15×10^{5}	0.36	−22.5	6.95×10^{5}	1.2×10^{4}	4.2
715-R15	65K	2000	10	1.48×10^{-9}(t)	0.22	−24.4	2.33×10^{5}	0.35	−22.8	1.5×10^{6}	1.24×10^{4}	4.1
715-R15	75K	2000	10	1.48×10^{-9}(t)	0.19	−24.9	4.01×10^{5}	0.3	−23.7	3.11×10^{5}	1.38×10^{4}	3.96
715-R15	85K	2000	10	1.48×10^{-9}(t)	0.23	−23.9	1.02×10^{5}	0.35	−22.6	1.37×10^{5}	1.2×10^{4}	4.31
715-R15	100K	2000	10	1.48×10^{-9}(t)	0.24	−23.6	7.71×10^{4}	0.37	−22	7.8×10^{4}	1.13×10^{4}	4.4
715-R15	120K	2000	10	1.48×10^{-9}(t)	0.24	−23.6	7.13×10^{4}	0.38	−22	7.23×10^{4}	1.12×10^{4}	4.42
715-R15	140K	2000	10	1.48×10^{-9}(t)	0.28	−22.7	3.99×10^{4}	0.42	−20.7	3.92×10^{4}	9.91×10^{3}	4.55
715-R15	160K	2000	10	1.48×10^{-9}(t)	0.28	−22.5	3.45×10^{4}	0.44	−20.7	3.99×10^{4}	9.47×10^{3}	4.52
715-R15	180K	2000	10	1.48×10^{-9}(t)	0.3	−22.2	2.57×10^{4}	0.46	−19.8	2.32×10^{4}	9.36×10^{3}	4.8
715-R15	200K	2000	10	1.48×10^{-9}(t)	0.31	−21.9	2.01×10^{4}	0.48	−19.4	1.98×10^{4}	9.12×10^{3}	4.9
715-R15	220K	2000	10	1.48×10^{-9}(t)	0.39	−20.6	9.87×10^{3}	0.61	−17.5	1.01×10^{4}	7.39×10^{3}	5.42
715-R15	240K	2000	10	1.48×10^{-9}(t)	0.39	−20.4	8.89×10^{3}	0.62	−17.1	9.03×10^{3}	7.35×10^{3}	5.46
715-R15	260K	2000	10	1.48×10^{-9}(t)	0.42	−20.1	7.23×10^{3}	0.65	−16.8	7.85×10^{3}	6.97×10^{3}	5.55
715-R15	280K	2000	10	1.48×10^{-9}(t)	0.43	−19.8	6.13×10^{3}	0.67	−16.4	6.77×10^{3}	6.77×10^{3}	5.61
715-R15	300K	2000	10	1.48×10^{-9}(t)	0.46	−19	4.22×10^{3}	0.72	−15.6	5.66×10^{3}	6.1×10^{3}	5.79
715-R15	320K	2000	10	1.48×10^{-9}(t)	0.47	−18.7	3.66×10^{3}	0.74	−15.2	5.05×10^{3}	5.67×10^{3}	5.83
715-R15	340K	2000	10	1.48×10^{-9}(t)	0.49	−17.9	3.09×10^{3}	0.81	−14.7	4.64×10^{3}	5.03×10^{3}	5.96
715-T12	15K	200	20	1.48×10^{-9}(t)	1.19	−16.8	1.67×10^{4}	1.06	−13	1.95×10^{3}	2.05×10^{3}	4.46
715-T12	25K	200	20	1.48×10^{-9}(t)	1.32	−15.1	2×10^{4}	1.23	−11.7	1.5×10^{3}	1.88×10^{3}	4.75
715-T12	35K	200	20	1.48×10^{-9}(t)	1.17	−17	1.76×10^{4}	1.03	−13.2	2.04×10^{3}	2.02×10^{3}	4.41
715-T12	45K	200	20	1.48×10^{-9}(t)	1.29	−15.5	2.13×10^{4}	1.19	−12.1	1.65×10^{3}	1.94×10^{3}	4.66
715-T12	55K	200	20	1.48×10^{-9}(t)	1.17	−17	1.77×10^{4}	1.05	−13.6	2.53×10^{3}	NA	4.31
715-T12	65K	200	20	1.48×10^{-9}(t)	1.3	−15.4	2.15×10^{4}	1.19	−12.6	2.75×10^{3}	1.82×10^{3}	4.64
715-T12	75K	200	20	1.48×10^{-9}(t)	1.18	−16.9	1.69×10^{4}	1.05	−13.1	1.93×10^{3}	2.25×10^{3}	4.47
715-T12	85K	200	20	1.48×10^{-9}(t)	1.31	−15	5.69×10^{4}	1.22	−11.8	1.61×10^{3}	2×10^{3}	4.78
715-T12	100K	200	20	1.48×10^{-9}(t)	1.34	−14.5	6.39×10^{4}	1.26	−11.5	2.27×10^{3}	1.94×10^{3}	4.69
715-T12	120K	200	20	1.48×10^{-9}(t)	1.3	−15	6.02×10^{4}	1.2	−11.6	1.63×10^{3}	1.81×10^{3}	4.79
715-T12	140K	200	20	1.48×10^{-9}(t)	1.3	−15.1	6.01×10^{4}	1.19	−11.6	1.65×10^{3}	1.94	4.77
715-T12	160K	200	20	1.48×10^{-9}(t)	1.33	−14.6	8.02×10^{4}	1.25	−11.3	2.25×10^{3}	1.9	4.74
715-T12	180K	200	20	1.48×10^{-9}(t)	1.33	−14.6	8.08×10^{4}	1.25	−11.4	2.27×10^{3}	1.9×10^{3}	4.73
715-T12	200K	200	20	1.48×10^{-9}(t)	1.37	−13.7	1.74×10^{4}	1.34	−11	1.92×10^{3}	1.97×10^{3}	4.96
715-T12	220K	200	20	1.48×10^{-9}(t)	1.44	−12.2	9.09×10^{3}	1.49	−10.3	3.84×10^{3}	1.78×10^{3}	5.03
715-T12	240K	200	20	1.48×10^{-9}(t)	1.47	−11.5	6.62×10^{3}	1.57	−10.1	7.89×10^{3}	1.9×10^{3}	4.93
715-T12	260K	200	20	1.48×10^{-9}(t)	1.48	−10.9	5.28×10^{3}	1.62	−9.92	7.32×10^{3}	1.84×10^{3}	5.13
715-T12	280K	200	20	1.48×10^{-9}(t)	1.5	−10.2	3.95×10^{3}	1.68	−9.56	6.41×10^{3}	1.78×10^{3}	5.4
715-T12	300K	200	20	1.48×10^{-9}(t)	1.5	−9.6	3.23×10^{3}	1.73	−9.43	5.86×10^{3}	1.8×10^{3}	5.58
715-T12	320K	200	20	1.48×10^{-9}(t)	1.52	−8.5	2.21×10^{3}	1.82	−9.07	4.6×10^{3}	1.72×10^{3}	5.97
715-T12	340K	200	20	1.48×10^{-9}(t)	1.53	−8.1	1.95×10^{3}	1.86	−8.96	4.17×10^{3}	1.68×10^{3}	6.12
715-T5	15K	200	50	1.48×10^{-9}(t)	2.09	−10	1.57×10^{4}	2.18	−14	4.09×10^{3}	5.13×10^{3}	4.4
715-T5	25K	200	50	1.48×10^{-9}(t)	2.08	−10	1.43×10^{4}	2.32	−14.6	2.4×10^{3}	3.21×10^{4}	4.4
715-T5	35K	200	50	1.48×10^{-9}(t)	1.98	−11.8	2.17×10^{4}	NA	NA	6.2×10^{3}	NA	NA
715-T5	45K	200	50	1.48×10^{-9}(t)	2.02	−10.3	1.67×10^{4}	1.63	−14.3	1.34×10^{3}	8.72×10^{4}	4.4
715-T16	55K	1000	50	1.48×10^{-9}(t)	2.32	−22	4.97×10^{5}	2.32	−18.2	5.12×10^{5}	7.47×10^{3}	NA
715-T16	65K	1000	50	1.48×10^{-9}(t)	2.32	−22	4.93×10^{5}	2.32	−18.2	5.5×10^{5}	7.59×10^{3}	NA
715-T16	75K	1000	50	1.48×10^{-9}(t)	2.44	−21.4	4.15×10^{5}	2.46	−17.7	1.34×10^{5}	7.31×10^{3}	3.2
715-T16	85K	1000	50	1.48×10^{-9}(t)	2.34	−21.5	3.42×10^{5}	2.36	−17.9	6.03×10^{4}	7.46×10^{3}	3.5
715-T16	100K	1000	50	1.48×10^{-9}(t)	2.49	−21.9	2.32×10^{5}	2.52	−17.4	3.28×10^{4}	6.86×10^{3}	3.78
715-T16	120K	1000	50	1.48×10^{-9}(t)	2.61	−20.3	1.74×10^{5}	2.64	−17.1	2.9×10^{4}	6.43×10^{3}	3.83
715-T16	140K	1000	50	1.48×10^{-9}(t)	2.6	−20.3	1.64×10^{5}	2.64	−16.9	2.69×10^{4}	6.43×10^{3}	3.88

715-T16	160K	1000	50	1.48×10^{-9}(t)	2.61	–20.3	1.64×10^{5}	2.65	–17	2.73×10^{4}	6.39×10^{3}	3.87
715-T16	180K	1000	50	1.48×10^{-9}(t)	2.62	–20.2	1.5×10^{5}	2.67	–17	2.56×10^{4}	6.36×10^{3}	3.92
715-T16	200K	1000	50	1.48×10^{-9}(t)	2.8	–19.3	9.19×10^{4}	2.87	–16.4	1.61×10^{4}	5.44×10^{3}	4.19
715-T16	220K	1000	50	1.48×10^{-9}(t)	3.03	–17.9	5.14×10^{4}	3.12	–15.9	1.14×10^{4}	4.24×10^{3}	4.5
715-T16	240K	1000	50	1.48×10^{-9}(t)	3.07	–17.5	4.28×10^{4}	3.19	–15.8	1.01×10^{4}	4.04×10^{3}	4.61
715-T16	260K	1000	50	1.48×10^{-9}(t)	3.11	–17.1	3.36×10^{4}	3.23	–15.6	8.88×10^{3}	3.68×10^{3}	4.75
715-T16	280K	1000	50	1.48×10^{-9}(t)	3.15	–16.5	2.53×10^{4}	NA	NA	NA	NA	NA
715-T16	300K	1000	50	1.48×10^{-9}(t)	3.18	–16.1	1.93×10^{4}	3.34	–15.4	8.53×10^{3}	3.25×10^{3}	5
715-T16	320K	1000	50	1.48×10^{-9}(t)	3.2	–15.1	1.27×10^{4}	3.39	–15.1	7.67×10^{3}	2.7×10^{3}	5.29
715-T16	340K	1000	50	1.48×10^{-9}(t)	3.22	–14.9	1.21×10^{4}	3.51	–15.2	7.02×10^{3}	2.8×10^{3}	5.34
715-R6	15K	1000	100	1.48×10^{-9}(t)	1.3	–15.9	1.64×10^{5}	1.38	–15.2	1×10^{5}	1.06×10^{4}	NA
715-R6	25K	1000	100	1.48×10^{-9}(t)	1.21	–16.3	2.08×10^{5}	1.14	–15.5	7×10^{4}	1.12×10^{4}	NA
715-R6	35K	1000	100	1.48×10^{-9}(t)	1.23	–16.8	2.3×10^{5}	1.33	–16.1	6.3×10^{4}	1.32×10^{4}	NA
715-R6	45K	1000	100	1.48×10^{-9}(t)	1.24	–16.6	2.1×10^{5}	1.35	–16	6.7×10^{4}	1.3×10^{4}	NA
715-R6	55K	1000	100	1.48×10^{-9}(t)	1.22	–16.9	2.34×10^{5}	1.32	–162.	6.1×10^{4}	1.33×10^{4}	NA
715-R6	65K	1000	100	1.48×10^{-9}(t)	1.32	–18	2×10^{5}	1.33	–15.9	6.7×10^{4}	1.22×10^{4}	NA
715-R6	75K	1000	100	1.48×10^{-9}(t)	1.28	–16.2	1.66×10^{5}	1.39	–15.8	8.2×10^{4}	1.22×10^{4}	NA
715-R6	85K	1000	100	1.48×10^{-9}(t)	1.22	–16.3	2.7×10^{5}	1.35	–16	5.8×10^{5}	1.3×10^{4}	NA
715-R6	100K	1000	100	1.48×10^{-9}(t)	1.25	–20.1	4.1×10^{5}	1.22	–168.	9.1×10^{4}	1.66×10^{4}	NA
715-R6	120K	1000	100	1.48×10^{-9}(t)	1.4	–18.2	2.37×10^{5}	1.37	–15.8	5×10^{5}	1.34×10^{4}	1.08
715-R6	140K	1000	100	1.48×10^{-9}(t)	1.47	–16.9	1.22×10^{5}	1.46	–15.1	1.2×10^{5}	1.14×10^{4}	2.43
715-R6	160K	1000	100	1.48×10^{-9}(t)	1.45	–17.4	1.78×10^{5}	1.42	–15.5	2.6×10^{5}	1.22×10^{4}	1.51
715-R6	180K	1000	100	1.48×10^{-9}(t)	1.46	–17	1.31×10^{5}	1.44	–15.2	2.2×10^{5}	1.17×10^{4}	2.29
715-R6	200K	1000	100	1.48×10^{-9}(t)	1.5	–16.3	9.65×10^{4}	NA	NA	NA	NA	NA
715-R6	220K	1000	100	1.48×10^{-9}(t)	1.52	–15.6	6.86×10^{4}	1.52	–14.7	1.7×10^{4}	9.6×10^{3}	3.63
715-R6	240K	1000	100	1.48×10^{-9}(t)	1.55	–14.6	4.37×10^{4}	1.57	–14.5	9.6×10^{3}	9.1×10^{3}	4.1
715-R6	260K	1000	100	1.48×10^{-9}(t)	1.64	–15.8	3.41×10^{4}	1.66	–14.9	9.7×10^{3}	1.22×10^{4}	4.26
715-R6	280K	1000	100	1.48×10^{-9}(t)	1.56	–13.7	2.67×10^{4}	1.59	–14.1	7.7×10^{3}	7.25×10^{3}	4.47
715-R6	300K	1000	100	1.48×10^{-9}(t)	1.57	–13.1	2×10^{4}	1.6	–14	6.2×10^{3}	6.76×10^{3}	4.72
715-R6	320K	1000	100	1.48×10^{-9}(t)	1.57	–12.5	1.54×10^{4}	1.61	–13.8	5×10^{3}	5.9×10^{3}	4.96
715-R6	340K	1000	100	1.48×10^{-9}(t)	1.56	–11.9	1.12×10^{4}	1.61	–1.36	4.3×10^{3}	5×10^{3}	5.19
715-T10	15K	500	200	1.48×10^{-9}(t)	4.97	–17.1	6.84×10^{4}	4.82	–17.8	3.03×10^{4}	5.35×10^{3}	NA
715-T10	25K	500	200	1.48×10^{-9}(t)	4.7	–18.6	1.47×10^{5}	4.36	–18.2	1.92×10^{4}	5.6×10^{3}	NA
715-T10	35K	500	200	1.48×10^{-9}(t)	4.87	–17.8	9.32×10^{4}	4.56	–17.7	2.25×10^{4}	5.06×10^{3}	NA
715-T10	45K	500	200	1.48×10^{-9}(t)	4.85	–17.8	9.4×10^{4}	4.57	–17.8	2.28×10^{4}	5.49×10^{3}	NA
715-T10	55K	500	200	1.48×10^{-9}(t)	4.54	–19.4	2.13×10^{5}	4.16	–18.7	1.64×10^{4}	6.84×10^{3}	NA
715-T10	65K	500	200	1.48×10^{-9}(t)	4.64	–18.9	1.62×10^{5}	4.3	–18.4	1.82×10^{4}	6.31×10^{3}	NA
715-T10	75K	500	200	1.48×10^{-9}(t)	4.78	–18.3	1.15×10^{5}	4.45	–17.9	2.03×10^{4}	5.48×10^{3}	NA
715-T10	85K	500	200	1.48×10^{-9}(t)	4.48	–19.3	2.1×10^{5}	4.11	–18.5	1.81×10^{4}	7.25×10^{3}	NA
715-T10	100K	500	200	1.48×10^{-9}(t)	4.66	–18.4	1.36×10^{5}	4.34	–17.9	2.11×10^{4}	6.25×10^{3}	NA
715-T10	120K	500	200	1.48×10^{-9}(t)	4.68	–18.3	1.28×10^{5}	4.36	–17.8	2.24×10^{4}	6.22×10^{3}	NA
715-T10	140K	500	200	1.48×10^{-9}(t)	4.84	–17.3	8.42×10^{4}	4.59	–17.3	3.53×10^{4}	5.91×10^{3}	NA
715-T10	160K	500	200	1.48×10^{-9}(t)	4.88	–17.1	8.04×10^{4}	4.62	–17.2	4.09×10^{4}	5.29×10^{3}	NA
715-T10	180K	500	200	1.48×10^{-9}(t)	4.86	–17.3	8.18×10^{4}	4.55	–17.4	3.84×10^{4}	4.77×10^{3}	NA
715-T10	200K	500	200	1.48×10^{-9}(t)	NA	NA	NA	NA	NA	NA	NA	NA
715-T10	220K	500	200	1.48×10^{-9}(t)	5.16	–15.1	3.17×10^{4}	5	–16.2	1.45×10^{4}	3.26×10^{3}	4.39
715-T10	240K	500	200	1.48×10^{-9}(t)	5.06	–15.3	2.8×10^{4}	5.06	–16.1	1.14×10^{4}	3.22×10^{3}	4.61
715-T10	260K	500	200	1.48×10^{-9}(t)	NA	NA	NA	NA	NA	NA	NA	NA
715-T10	280K	500	200	1.48×10^{-9}(t)	5.18	–14.2	1.99×10^{4}	5.15	–15.8	1.02×10^{4}	2.77×10^{3}	4.92
715-T10	300K	500	200	1.48×10^{-9}(t)	5.19	–13.8	1.58×10^{4}	5.17	–15.5	8.17×10^{3}	2.36×10^{3}	5.15
715-T10	320K	500	200	1.48×10^{-9}(t)	5.18	–13.3	1.16×10^{4}	NA	NA	6.73×10^{3}	NA	NA
715-T10	340K	500	200	1.48×10^{-9}(t)	5.17	–13.1	1×10^{4}	5.22	–15.2	6.26×10^{3}	1.82×10^{3}	5.55

For C_i, "t" represents the value calculated from the technological dielectric thickness and theoretical permittivity. One may notice that the mobility by conventional method in saturation regime decreases with temperature, this is because the poor linearity in $I_{Dsat}^{0.5}(V_G)$ at low temperature and its linearity is improved with heating, similar tendency can be observed for the threshold voltage. However, this issue is free in the Y function method.

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Chapter 4
Modeling

Modeling is the key work of this thesis. The previous characterizations give us an intuitive understanding of the OFETs' I-V characteristics, modeling will theoretically enables a deep insight into the OFETs' operating mechanism, the carrier transport, the determinants of parameters and their inherent relationships. In this chapter, we shall first present a modeling on the OFETs' I-V characteristics in which a semi-analytical solution for Poisson's equation is developed. Due to the significant influences of traps, a charge trapping study by simulation is also performed. Next, we move to the carrier transport modeling with the results of low-temperature measurements on a set of TIPS-pentacene OFETs. And finally, a theoretical analysis of OFETs' carrier mobility is proposed.

4.1 OFETS' I-V CHARACTERISTICS MODELING (*based on the paper published in Journal of Applied Physics,* ***110****, 014510,* 2011)[1]

4.1.1 INTRODUCTION

Organic electronic attracts much interest from current microelectronics industries because of its special features such as large area, flexible, easy to fabricate and low cost. As an important type of devices in such a booming stream, organic field-effect transistors (OFETs), however, are not very well understood as compared to the classical inorganic counterparts. Up to now, a number of works have contributed to the OFETs' modeling, regarding e.g. carrier transport,[2, 3] (dc) electrical characteristics,[4-10] device parameters[11-14] and low-frequency noise[15] etc. With regard to the dc modeling, the presently published works are mostly based on the conventional I-V relationships taking into account the parameters variations and/or dependences, there are few dc models which originate from the Poisson equation solution,[4] as it is done for the classical silicon MOSFETs. Therefore, those models cannot very explicitly describe the potential distribution and thus the charge density in the organic film. In examining the existing difficulties, one can find three main factors. First, the organic materials utilized as semiconductor are usually intrinsic due to the very weak Van der Waals force interacting between the adjacent molecules.[16] The charge transport in this kind of media, of course, is different from that in crystalline silicon. Second, the contact is a severe limitation in OFETs.[17] It usually concerns a charge injection barrier from a metal contact into organic materials,[18] revealing large contact resistances.[19] Third, a large number of traps significantly affect the OFETs' characteristics.[13, 20] They might reside at the interfaces,[4, 21] at the grain boundaries,[2] in the organic film[22] and in the contact region as well.[17] The presence of traps modifies the main OFET parameters, such as threshold voltage,[23] mobility,[24] contact resistance,[17] subthreshold slope[25, 26] as well as low-frequency noise properties. This modification causes a large dispersion in parameters from device-to-device, making it hard to estimate the OFETs' performance.[27]

In this paper, we first introduce the one-dimensional (1-D) Poisson equation solution for the organic-dielectric-gate structure, by which the potential profile in the organic film at each gate voltage is derived. And then, the model is applied to our pentacene OFETs and a good agreement with experimental data is obtained. However, we observe a large discrepancy in the application to TIPS-pentacene OFETs due to the presence of traps. By numerical simulation, we separately investigate the effects of interface states, surface/bulk traps, donor /acceptor-like

traps, at a single energy level and of uniform energy distribution. Finally, a close fitting to experimental data is achieved including the influence of traps.

4.1.2 1-D ANALYTICAL SOLUTION OF POISSON'S EQUATION

A. For intrinsic organic semiconductors

Organic semiconductors are generally intrinsic, i.e., the free carrier density in such media is very low. At the first step, we consider a trap-free condition; the influences of traps will be discussed later. Unlike previous works,[4] we remark that the organic transistors are usually open surface-configured, which means that the surface of organic film opposite to the gate dielectric is free, and, by turn, the potential at this surface, in fact, is not fixed (e.g. to zero). This assumption is always valid since this surface is either exposed in the air without passivation in the case of bottom-gate configuration, or adjacent to the very thick substrate compared to the relatively thin film of organic semiconductor in the case of top-gate configuration. Therefore, a one dimensional (1-D) Poisson's equation solution can be introduced into the organic transistors. This solution was first established by Taur,[28] for the undoped or lightly-doped double-gate MOSFETs, in which the low doping and the half part of symmetric double-gate structure are exactly identical to the organic transistors in spite of the two different kinds of semiconductors: silicon and organic materials.

The schematic band diagrams of organic semiconductor-dielectric-gate structure are shown in Fig. 4.1, independently of bottom/top-gate and bottom/top-contact configurations. For simplicity, an n-type semiconductor is chosen for the following discussion, the adaptation to p-type transistor is straightforward. As shown in Fig. 4.1a, when a zero gate voltage is applied, the bands of organic semiconductor (OSC) are flat throughout the film thickness due to the intrinsic semiconductor and the negligible depletion charge. The Fermi level of OSC is in the middle of band gap, namely $E_F \approx E_{Fi}$. The position of system Fermi level is determined by the work function of gate electrode. Since there is no contact to the OSC body, the energy levels are referenced to the Fermi level of source/drain electrode, usually a metal, as indicated by the dotted line. Also for simplicity, the difference between the gate work function (Φ_{mG}) and the organic Fermi level (E_F) is assumed to be zero, in addition, the source/drain Fermi level (Φ_{mC}) and E_F are also assumed to be equal. In fact, the former difference will shift the flat-band voltage and thus the threshold voltage, and the latter one will alter the charge injection barrier and consequently the contact resistance.[19]

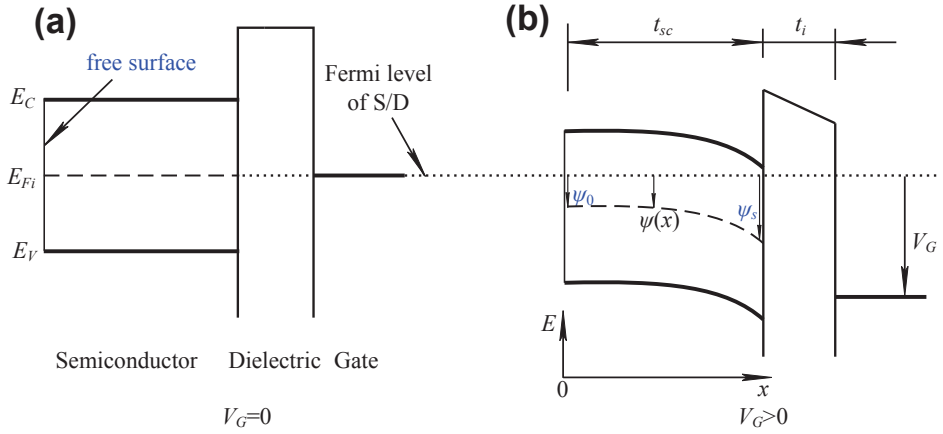


Figure 4.1 | Band diagrams of organic-dielectric-gate structure. (a) At zero gate voltage, the bands of semiconductor are flat throughout all the film thickness. The energy levels are referenced to the Fermi level of source/drain (dotted line). (b) At a higher gate voltage, the semiconductor bands shift entirely downward and the bands of semiconductor near dielectric are bent. Note that the potential at free surface is not fixed to zero but rather increases with the gate bias.

At a positive gate voltage as seen in Fig. 4.1b, the bands of OSC are globally put downward because of the floating potential at such an open surface and low charge density, the OSC enters into a volume (weak) accumulation or inversion. The Fermi level moves toward the conduction band, implying that the OSC now is n-type conducting. As the gate voltage is increased sufficiently, e.g. V_G beyond the nominal threshold voltage (V_T), more electrons are induced. As discussed below, the surface potential adjacent to the gate dielectric increases more quickly and next decouples with the opposite one, hence the OSC bands near dielectric are bent. In transistors, the conduction band moves downward closer to the Fermi level of source/drain contacts, large numbers of electrons are injected from the source and/or drain electrode into the organic conducting film, where a superficial accumulation occurs. In the following text, we will still employ the conventional terms of conduction band and valence band, their edges corresponds to the LUMO (lowest unoccupied molecular orbital) and the HOMO (highest occupied molecular orbital) for organic semiconductor, respectively.

As seen in Fig. 4.1b, the surface potential on two sides of organic film are defined as ψ_0 and ψ_s, where ψ_s is for that at the surface close to the dielectric (channel surface). With the coordinates defined in this figure, one can write Poisson's equation for the OSC film with only the mobile charge (electron here) density as:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{sc}} n_i e^{q\psi/kT} \tag{4.1}$$

where q is the electronic charge, ε_{sc} is the permittivity of organic semiconductor, n_i is the intrinsic carrier density, and kT is the thermal energy. Because we consider a n-type OSC with $q\psi/kT>>1$, the hole density is thus negligible. Note that the intrinsic carrier density is determined by $n_i^2=N_cN_v\exp(-E_g/kT)$, with N_c and N_v being the effective density of states in the conduction band (or LUMO) and valence band (or HOMO), respectively; E_g is the bandgap energy. Owing to the large E_g in organic semiconductors, n_i is usually very small in the rang of 10^5-$10^6/\text{cm}^3$ with N_c and N_v around of $10^{21}/\text{cm}^3$.[4, 22]

With the boundary condition $d\psi/dx|_{x=0}=0$, one can integrate Eq. 4.1 for whole film thickness as:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{sc}}\left(e^{q\psi/kT} - e^{q\psi_0/kT}\right)} \tag{4.2}$$

where ψ_0 is the surface potential at the free surface. Integrating one more time, one obtains the potential as a function of x:

$$\frac{q(\psi-\psi_0)}{2kT} = -\ln\left[\cos\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{sc}kT}}e^{q\psi_0/2kT}x\right)\right] \tag{4.3}$$

Hence the surface potential $\psi_s\equiv\psi(x=t_{sc})$ is given by

$$\frac{q(\psi_s-\psi_0)}{2kT} = -\ln\left[\cos\left(\sqrt{\frac{q^2n_i}{2\varepsilon_{sc}kT}}e^{q\psi_0/2kT}t_{sc}\right)\right] \tag{4.4}$$

The two potentials ψ_0 and ψ_s are related to V_G, and they can be solved by the boundary condition at the OSC-dielectric interfaces for each V_G with the coupled equation 4.4:

$$\varepsilon_i\frac{V_G-\psi_s}{t_i} = \varepsilon_{sc}\left.\frac{d\psi}{dx}\right|_{x=t_{sc}} = \sqrt{2\varepsilon_{sc}kT\left(e^{q\psi_s/kT} - e^{q\psi_0/kT}\right)} \tag{4.5}$$

where ε_i and t_i are the permittivity and the thickness of the gate dielectric, respectively.

Equations 4.4 and 4.5 provide a system solution for 1-D Poisson's equation and can exactly describe the potential distribution in the organic film for each gate voltage. It can be solved numerically by using a simple root equation finder in mathematical software. Sometimes, organic semiconductors might be lightly doped by deliberate doping or unforeseen contamination. Hence, the doping effect is discussed below.

B. For lightly doped organic semiconductors

With the same schematic as in Fig. 4.1, the Poisson equation reads as:[29]

$$\Delta\psi(x) = -q\left[p(x) - n(x) + N_d - N_a\right]/\varepsilon_{sc} \tag{4.6}$$

where Δ is the Laplace operator, $p(x)$ is the hole density, $n(x)$ is the electron density, N_d and N_a are the density of donor and acceptor impurities, respectively. Here suppose a slightly p-type doped semiconductor, the doping level is low thus the Fermi level is not significantly shifted away from its intrinsic value. As a result, the nominal inversion and accumulation are nearly symmetric. At zero gate voltage, $p(x)=N_a$ and $n(x)=n_i^2/N_a$. As a positive gate voltage is applied, according to the Boltzmann approximation: $p(x)=N_a\exp(-q\psi/kT)$ and $n(x)=(n_i^2/N_a)\exp(q\psi/kT)$, the Poisson equation and the boundary conditions can be rewritten as:

$$\begin{aligned}
&\Delta\psi(x) = \frac{qN_a}{\varepsilon_{sc}}\left\{1 - \exp\left(-\frac{q\psi}{kT}\right) + \left(\frac{n_i}{N_a}\right)^2\left[\exp\left(\frac{q\psi}{kT}\right) - 1\right]\right\} \\
&\psi = \psi_s, \qquad d\psi/dx = -C_i(V_G - V_{fb} - \psi_s)/\varepsilon_{sc}, \quad x = t_{sc} \\
&\psi = \psi_0, \qquad d\psi/dx = 0, \qquad\qquad\qquad\quad x = 0
\end{aligned} \tag{4.7}$$

where C_i is the unit area capacitance of the gate dielectric, and V_{fb} is the flat-band voltage.

To solve Eq. 4.7, one can multiply $d^2\psi/dx^2$ on both sides and integrate it for all the film thickness, and thus obtaining:

$$\begin{aligned}
\frac{d\psi}{dx} = \Bigg\{ &\frac{2qN_a}{\varepsilon_{sc}}\left\{\left[\psi - \psi_0 + \frac{kT}{q}\exp\left(-\frac{q\psi_0}{kT}\right) - \frac{kT}{q}\exp\left(-\frac{q\psi}{kT}\right)\right]\right. \\
&\left.+\left(\frac{n_i}{N_a}\right)^2\left\{\left[\psi_0 - \psi + \frac{kT}{q}\exp\left(\frac{q\psi}{kT}\right) - \frac{kT}{q}\exp\left(\frac{q\psi_0}{kT}\right)\right]\right\}\right\}^{1/2}
\end{aligned} \tag{4.8}$$

Because this is a nonlinear function, it can be solved only by approximation. For the sake of clarity we discuss it in two regions: weak inversion and strong inversion. The term of inversion is kept here, but it is not strictly defined as stated above.

In the case of *weak inversion*, $\psi_f < \psi < 2\psi_f$ and $\psi >> kT/q$, where $\psi_f = kT/q\ \ln(N_a/n_i)$, Eq. 4.8 can be rewritten as:[29]

$$\frac{d\psi}{dx} = \sqrt{\frac{2qN_a}{\varepsilon_{sc}}(\psi - \psi_0)\left[1 - \left(\frac{n_i}{N_a}\right)^2\right]} \tag{4.9}$$

and the final integration gives:

$$\psi = \psi_0 + (\psi_s - \psi_0)\left\{1 + \sqrt{\frac{qN_a}{2(\psi_s - \psi_0)\varepsilon_{sc}}\left[1 - \left(\frac{n_i}{N_a}\right)^2\right]}(x - t_{sc})\right\} \tag{4.10}$$

In the case of *strong inversion*, $0 < kT << \psi - 2\psi_f$, Eq. 4.8 can be rewritten as:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTN_a}{\varepsilon_{sc}}\left(\frac{n_i}{N_a}\right)^2\left[\exp\left(\frac{q\psi}{kT}\right) - \exp\left(\frac{q\psi_0}{kT}\right)\right]} \tag{4.11}$$

and the final integration provides:

$$\psi = \psi_0 - \frac{kT}{q}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i^{\,2}}{2kT\varepsilon_{sc}N_a}}\exp\left(\frac{q\psi_0}{2kT}\right)x\right]^2\right\} \tag{4.12}$$

This solution supplements the doping level N_a but approximations are required, hence this is not a fully analytical solution. However, the doping level doesn't significantly affect the real solution results (as shown by numerical simulation, not displayed here), and in addition we can see that, if $N_a \approx n_i$ the second solution will return to the previous one.

C. Derivation of the charge density and the drain current

Upon the above considerations, the potential profile and the charge density can be derived. As we know, each gate voltage corresponds to a potential profile and the total induced charge per unit surface in the organic film can be calculated by Gauss's law:

$$Q_i(\psi_0,\psi_s)=\frac{d\psi}{dx}\varepsilon_{sc} \tag{4.13}$$

Moreover, based on the charge neutrality in this structure, we have:

$$V_G=V_{fb}+\psi_s+\frac{Q_i(\psi_0,\psi_s)}{C_i}+\frac{qN_{ss0}\psi_0}{C_i}+\frac{qN_{ss}\psi_s}{C_i}-\frac{Q_{fix}}{C_i} \tag{4.14}$$

where N_{ss0} and N_{ss} are the surface state density ($1/\mathrm{eVcm^2}$) at the surfaces corresponding to ψ_0 and ψ_s, respectively. Q_{fix} is the fixed charge ($\mathrm{q/cm^2}$) which in principle is distributed at the OSC-dielectric interface, its impact is usually included in the flat-band voltage. Associating Eqs.4.9-4.14, one can solve ψ_0 and ψ_s for each V_G, and subsequently $Q_i(V_G)$ according to Eq. 4.13. Here the surface states on both sides and the fixed charge is considered, the former would affect the form of the subthreshold characteristics(C-V and I-V) and the latter would change the position of C-V and I-V characteristics against the gate voltage, and thus shift the threshold voltage.

Having Q_i, the transfer characteristics of organic transistors in *linear regime* can be obtained as:

$$I_D(V_G)=\frac{W}{L}\mu_{eff}Q_i(V_G)\times V_D \tag{4.15}$$

where W and L are the channel width and length, respectively, μ_{eff} is the effective mobility usually measured at small drain voltages, and V_D is the drain voltage.

4.1.3 EXPRIMENTAL RESULTS AND DISCUSSIONS

A. Pentacene OFETs

The previous model was used to fit the experimental characteristics of a set of top-contact (TC) and bottom-gate (BG) pentacene OFETs. The parameters are summarized in Table 4.1, the flat-band voltage is assumed to be equal to the gate-semiconductor work function difference. Because its value is very small, sometimes it could be neglected. All OFETs exhibited good field-effect transistor behaviors during this study, non-linear contact resistance at small drain voltages were not observed, more details about electrical characteristics can be found in ref.[30]

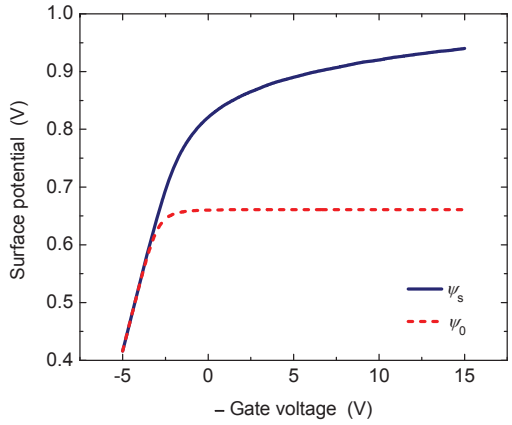


Figure 4.2 | Surface potentials at both sides of the organic film, in which a small flat-band voltage V_{fb}=0.14V was assumed. At small V_G, both potentials increase as the same trend, indicating the volume inversion. However at higher V_G, the potential at free surface saturates and the other one still increases a little with V_G.

As seen in Fig.4.2, ψ_0 and ψ_s rise with V_G but there are some features worthy of attention: **1**, At small V_G, the two potentials increase as a same trend, i.e. $\psi_0 \approx \psi_s$. This is because of the globally shifted bands of OSC in volume inversion (or accumulation). Hence the total charge in the film is proportional to the film thickness. **2**, At V_G above V_T, the induced charges are attracted by the gate electrical field and become more concentrated toward the OSC-dielectric interface. These quasi-surface charges of high density screen the gate field from the center of organic film, ψ_0 and ψ_s are getting decoupled. This result can be also expected from Eqs 4.4, 4.5 or 4.12. Since the angle of the cosine function in Eqs.4.4 and 4.12 cannot exceed $\pi/2$ to ensure the positive variable region in ln

function, ψ_0 reaches its maximum of $(kT/q)\ln(\pi^2\varepsilon_{sc}kT/2q^2n_it_{sc}^2)$ in Eq.4.4, similarly for Eq. 4.12. However ψ_s still slightly increases with V_G, cf. Eq. 4.5.[29] Increasing V_G further, the charge density will increase linearly with V_G and the charge screening becomes more and more pronounced. The charge carriers are almost distributed in the layers in close vicinity of the dielectric, a superficial charge transport appears. In this case, the overall charge no longer depends on the film thickness.

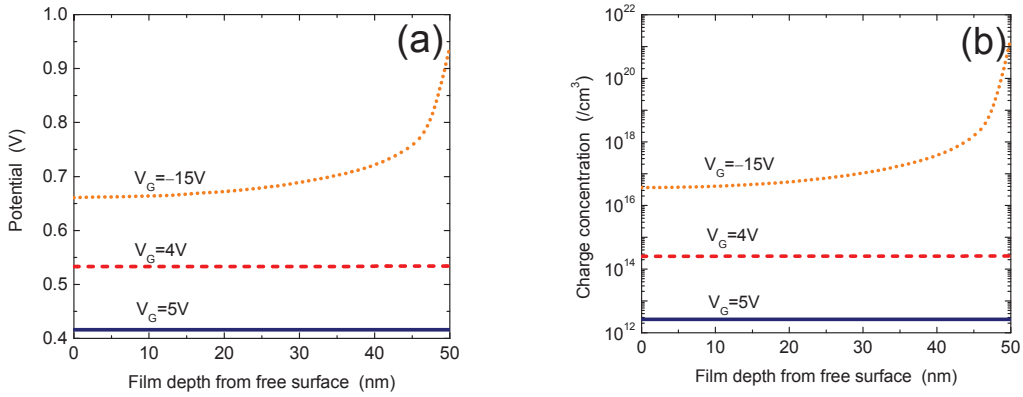


Figure 4.3 | Potential profile (a) and charge concentration (b) in the organic film for various gate voltages. Note the variation at the free surface as well as the tail in the bulk.

The potential profile and the charge concentration in organic film are shown in Figs.4.3a and 4.3b, respectively, for three gate voltages. ψ_0 saturates quickly with V_G but ψ_s still increases a little. More importantly, one can find that in Fig. 4.3b, the charge concentration in the layers adjacent to the dielectric is significantly enhanced by V_G, from $10^{12}/\text{cm}^3$ (V_G=5V) to $10^{21}/\text{cm}^3$ (V_G=−15V). For all the film thickness, at small V_G the charge distribution is uniform, however at high V_G the charge concentration is not constant, with a large difference of 5 orders of magnitude from free surface to the other side. This result is also in agreement with the literature,[31, 32] the accumulation layer only extends to a few nanometers into the bulk at high gate voltages. Meanwhile, it should be noted that the tail of charge concentration in the bulk is also significantly modulated by V_G, from $10^{12}/\text{cm}^3$ (V_G=5V) to $10^{16}/\text{cm}^3$ (V_G=−15V) for the layers close to the *free surface*. Similar feature had been applied to elucidate the gate-voltage dependence of contact resistance by Richards *et al.*[33] The bulk conductivity is also dependent of the gate voltage, partially leading to the gate-voltage dependence of contact resistance, especially in the staggered OFETs. To confirm these discussions, a charge centroid diagram is shown in Fig. 4.4. At V_G below 0V, the charge centroid is in the middle of OSC layer, implying uniform charge distribution, however at greater V_G, the centroid moves quickly to the layers next to the dielectric, indicating a superficial charge distribution.

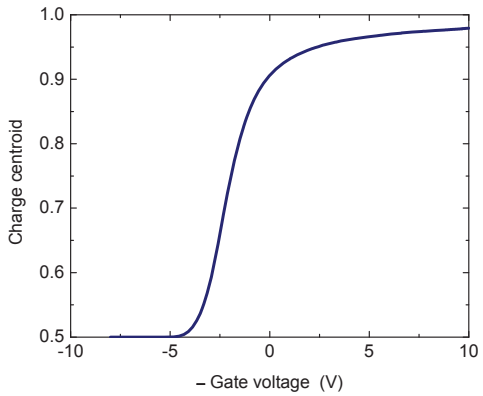


Figure 4.4 | Charge centroid of the organic film as a function of gate voltage. At small V_G, the centroid is in the center of film, implying a uniform charge distribution. As V_G increases, the centroid moves quickly to the surface adjacent to the dielectric, implying a superficial charge transport.

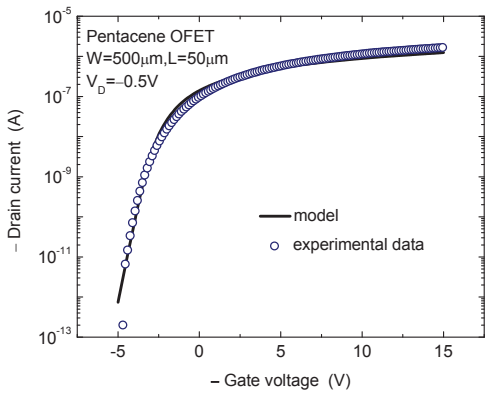


Figure 4.5 | Comparison of the experimentally measured transfer characteristics in linear regime with the calculation by modeling. Here the measurement data are contact-resistance corrected, N_{ss}=3×10^{12}/eVcm^2, N_{ss0}=0 and negative Q_{fix}=6.4×10^{-7} C/cm^2.

According to Eq. 4.15, the drain current is calculated by this quasi-analytical solution and is compared with the transfer characteristics (in linear regime) measured in an OFET, as shown in Fig. 4.5. Here W=500μm, L=50μm, and V_D=−0.5V. Because the previous analysis did not consider the contact resistance and the gate-voltage dependence of effective mobility, hence such a theoretical solution should take them into account to fit the raw measurement data. A contact resistance of R_{sd}=5.5×10^{4}Ω was extracted previously by Y function method,[30] and a contact resistance-free effective mobility was found to be nearly constant with V_G in strong accumulation, namely $\mu_{eff}\approx\mu_0$=0.26cm^2/Vs. In order to obtain a good fitting, the following parameters were employed, N_{ss}=3.3×10^{12}/eVcm^2, N_{ss0}=0 and negative Q_{fix}=6.4×10^{-7} C/cm^2. Note that N_{ss0}=0 doesn't mean no effect from the free surface since in subthreshold region, the charge trapping from the interface states on both sides are similar because of the volume transport. Moreover, ψ_0 saturates above threshold, it doesn't affect the carrier transport at high gate biases. In short, the effective impact of N_{ss0} on the subthreshold characteristics is actually included in N_{ss}. Interestingly, this N_{ss} value is consistent with our results yielded previously by the subthreshold slope technique[23] and by the low-frequency noise measurements.[34] Finally, from this figure one can find a close fitting not only in subthreshold region but also in high gate-bias region, confirming the validity of the applied model.

B. TIPS-pentacene OFETs

This method is next applied to a group of top-gate (TG) and bottom-contact (BC) TIPS-pentacene OFETs, the parameters are summarized in Table 4.2, more details for device fabrication and characterization can be found in ref.[35] We selected one OFET to illustrate the results, W=200μm, L=50μm. Here V_D=−0.2V, $\mu_{eff}\approx\mu_0$=2.6cm^2/Vs, R_{sd}=1.4×10^{5}Ω. For clarity, the same processes like the above are directly shown in Fig. 4.6 and one can observe similar results. Now we focus on the drain current comparison, where a large deviation in subthreshold region arises as seen in Fig. 4.7. Such a deviation cannot be eliminated by a simple fitting with given surface states and fixed charges. For this fitting, N_{ss}=4×10^{11}/eVcm^2, N_{ss0}=0 and negative Q_{fix}=2.8×10^{-8} C/cm^2 were used.

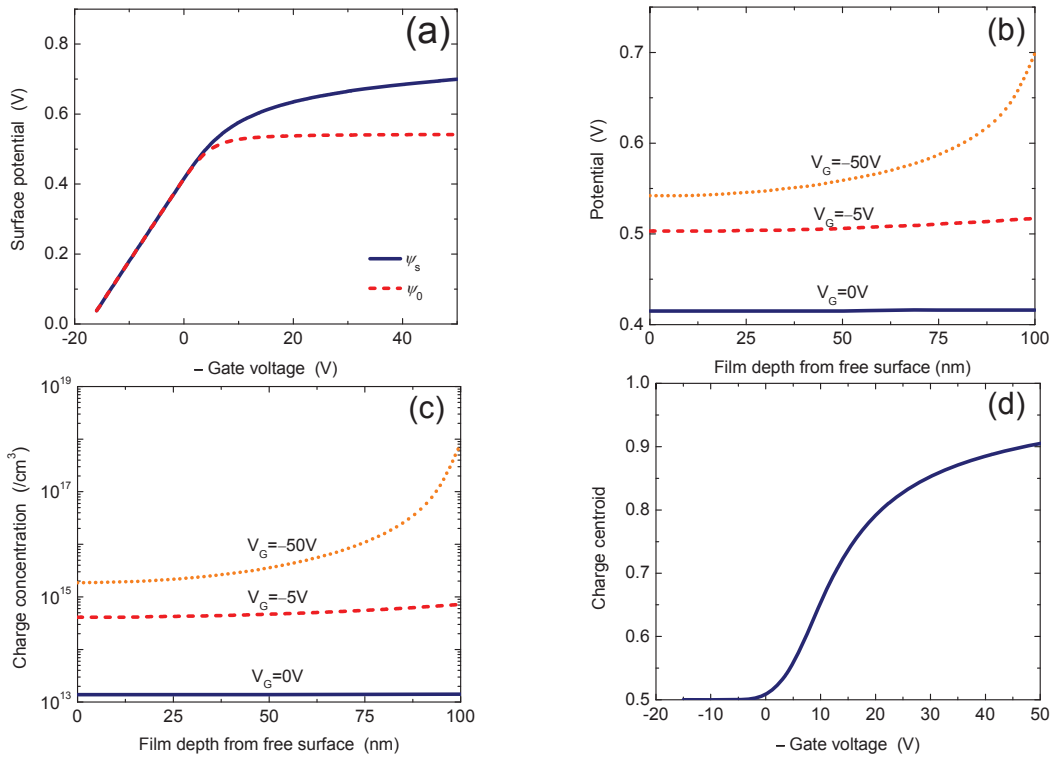


Figure 4.6 | The same process of Figs. 2-4 applied to the TIPS-pentacene OFETs, in which a small flat-band voltage V_{fb}=0.46V was assumed.

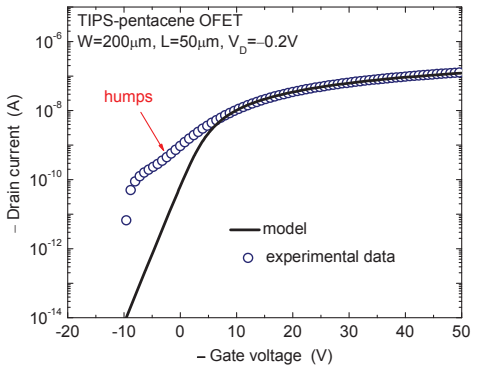


Figure 4.7 | Comparison of the transfer characteristics for a TIPS-pentacene OFET with the calculation. A clear deviation in the subthreshold region was observed, one can find a hump that cannot be fitted by the analytical model with considering the surface states and the fixed charges, here N_{ss}=4×10^{11}/eVcm^2, N_{ss0}=0 and negative Q_{fix}=2.8×10^{-8} C/cm^2.

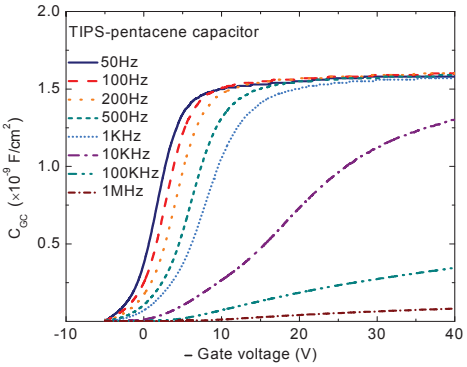


Figure 4.8 | C-V characteristics of a simultaneously fabricated capacitor at various frequencies. The C-V curves converge at low frequencies, hence the data at f=50Hz are used for further analysis.

TABLE 4.1 Parameters used for pentacene OFETs

Temperature	T	300	(K)
Boltzmann's constant	k	1.38×10^{-23}	(J/K)
Band density of states	N_c, N_v	10^{21}	(cm^{-3})
Bandgap energy	E_g	1.85	(eV)
Electron affinity	χ_e	3.2	(eV)
Ionization energy	χ_p=χ_e+E_g	5.05	(eV)
Semiconductor permittivity	$\varepsilon_{sc}/\varepsilon_0$	3.5	...
Dielectric permittivity(SiO$_2$)	$\varepsilon_i/\varepsilon_0$	3.9	...
Semiconductor thickness	t_{sc}	50	(nm)
Dielectric thickness	t_i	50	(nm)
Gate work function(p+Si)	Φ_{mG}	5.1	(eV)
Source/drain work function(copper)	Φ_{mC}	4.65	(eV)
Gate/OSC work function difference	Φ_{mG}–(χ_e+E_g/2)	0.525	(eV)
Unit area capacitance of dielectric	C_i	7×10^{-8}	(F/cm^2)

TABLE 4.2 Parameters used for TIPS-pentacene OFETs

Temperature	T	300	(K)
Boltzmann's constant	k	1.38×10^{-23}	(J/K)
Band density of states	N_c, N_v	2×10^{21}	(cm^{-3})
Bandgap energy	E_g	1.8	(eV)
Electron affinity	χ_e	2.9	(eV)
Ionization energy	χ_p=χ_e+E_g	4.7	(eV)
Semiconductor permittivity	$\varepsilon_{sc}/\varepsilon_0$	4	...
Dielectric permittivity(Cytop^{TM})	$\varepsilon_i/\varepsilon_0$	2.1	...
Semiconductor thickness	t_{sc}	100	(nm)
Dielectric thickness	t_i	1.2	(μm)
Gate work function(Ag)	Φ_{mG}	4.26	(eV)
Source/drain work function(Au)	Φ_{mC}	5	(eV)
Gate/OSC work function difference	Φ_{mG}–(χ_e+E_g/2)	0.46	(eV)
Unit area capacitance of dielectric	C_i	1.48×10^{-9}	(F/cm^2)

To explore further these properties, we examined the capacitance-voltage(C-V) behaviors of a simultaneously fabricated capacitor on the same substrate; its parameters are identical to other OFETs. In Fig. 4.8, the capacitance per unit area with respect to the bias voltage varies with frequency. This is known to be due to the interface states and/or traps. At small enough frequency of applied AC signal,[15, 36, 37] the carriers can be captured by the interface states and/or the traps, which are located at the surfaces and/or in the bulk. As the frequency is increased, they may have not enough time to be captured, hence they cannot respond to the C-V characteristics. As a result, smaller capacitance is observed at higher frequencies, for a fixed bias. This phenomenon is only significant below the threshold where the charge density is very low and comparable to the trap density.[25] So, a substantial portion of charge carriers undergo a trapping process, whereas above the threshold, due to the previous trap-filling and the relatively much greater number of charge carriers relative to the traps, such a trapping impact is much less pronounced, as seen in Fig. 4.8. From these results we can see that, the C-V characteristics reflect the charge in the semiconductor including the trapped charge and the free charge.

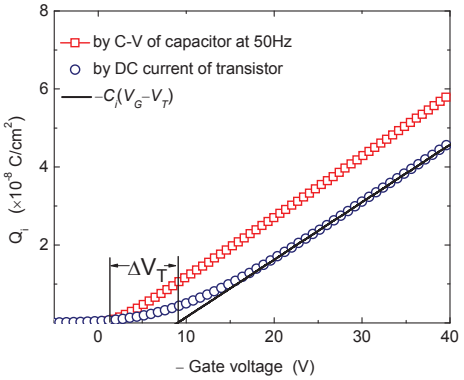


Figure 4.9 | Charge density per unit area obtained by the C-V characteristics of the capacitor (at f=50Hz), or obtained by the static drain current (in linear regime) measured from a transistor. The solid line represents the charge approximation at strong accumulation. The difference of charge threshold voltage between the C-V and DC characteristics (ΔV_T) reflects the trapped charges.

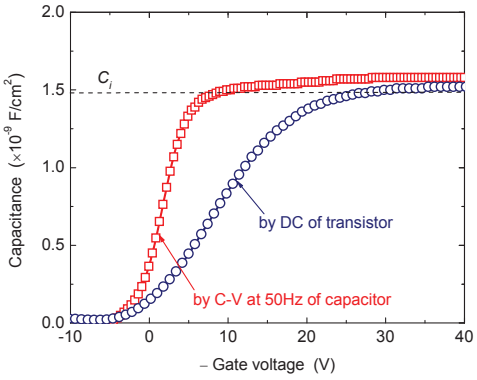


Figure 4.10 | Comparison of C-V characteristics between the raw data (capacitor) and the quasi-static one calculated by DC current (transistor). The much steeper slope of raw C-V data implies the trapped charges which respond to the C-V characteristics but do not contribute to the current.

The split C-V technique is thus applied to obtain the overall charge, as shown in Fig. 4.9.[38] Here we chose the data at f=50Hz because the C-V curves converge at low frequencies, where nearly all the traps could respond. The integrated charge of this capacitor is then compared to the charge calculated from the drain current (contact resistance corrected) in linear regime of that OFET, according to Eq. 4.15. Note that the C-V data of the capacitor represent better the OFETs' intrinsic C-V characteristics since a variety of additional effects existing in OFETs severely affect their electrical properties. From this figure one can find a clear difference: the charge by C-V data is larger than that by DC data, or from another point of view, the charge threshold for C-V is less than that for DC. This is due to the fact that the charge from DC characteristics represents only the free charge. It is certainly less than the C-V charge which incorporates not only the free charge but also the trapped one. Therefore, one could roughly estimate the trapped charge per unit area from the difference seen in Fig. 4.9 by means of:[23]

$$Q_t = C_i \Delta V_T \tag{4.16}$$

Here ΔV_T=9V, corresponds to the trapped charges Q_t=1.33×10^{-8} C/cm^2 or the equivalent surface trap density N_t=Q_t/q= 8.3×10^{10} /eVcm^2 in this transistor.

Furthermore, we calculated the C-V characteristics from quasi-static data (contact corrected) by the equation:

$$C_{gc}(V_G) = \frac{\partial Q_i(V_G)}{\partial V_G} = \frac{\partial I_D(V_G)}{\partial V_G}\frac{L}{W\mu_{eff}V_D} = g_m(V_G)\frac{L}{W\mu_{eff}V_D} \tag{4.17}$$

This quasi-static C-V is compared to the raw measurement C-V, as shown in Fig. 4.10. One can also observe a difference: for the quasi-static C-V, it rises slower than the experimental C-V as sweeping the bias from positive to negative values. This is because the first induced charge carriers are nearly captured by traps, these trapped charge carriers respond to C-V but very few mobile charge carriers contribute to the current. After the traps are filled, free charge carriers are buildup and a clear current emerges. That's why the charge threshold for C-V is smaller (or earlier) than that for DC current, cf. Fig. 4.9. A similar feature has been discussed by Horowitz *et al.*[4] in his pioneering work on modeling, and later applied to explain the threshold voltage extraction in his associated work,[25] where a mobility threshold is defined once the free carrier density becomes higher than the trapped carrier density.

It must be stressed that the above model may not have analytical solution if we add the bulk traps. However, the bulk traps is an important factor to interpret the experimental I-V and C-V characteristics, particularly around the threshold voltage. In consequence, we solve numerically the Poisson equation with bulk traps by using the finite element method.

4.1.4 TRAPS

A. Electronic traps

The electronic traps widely populate in organic transistors, at surfaces and in the bulk. They could be simply classified as acceptor-like traps and donor-like traps. An acceptor-like trap is negatively charged if filled with an electron and neutral if empty. For a donor-like trap, it is neutral when filled by an electron and becomes positive if empty. Traps may originate from impurities, external contamination and structural defects,[24, 39] their energy levels that have an impact on electrical properties are within the bandgap with density of states (DOS) as discrete levels, [4, 21, 26] Gaussian distribution[2, 10] or exponential distribution etc.[22, 40] In general, acceptor states are located in the upper half of the bandgap and donor states can be found in the lower half of the bandgap. Their charging/discharging is similar to interface traps and depends on the position of Fermi level with regard to their energy levels.

If the applied gate bias is zero and the energies of the states are close to the conduction or valence bands (e.g., few kT from the band edge), the carriers can enter into and escape out of these states by thermal activation process, these states are referred to as traps. If their allowed energies are far from the bands, these states are usually referred to as generation-recombination (G-R) centers. The former are also often called shallow traps and the latter are called deep traps. Note that, due to the intrinsic organic semiconductors and open surface in OFETs, increasing the gate bias, the conventional deep traps (not in the opposite half of bandgap) will be filled earlier than the nominal shallow traps,[4] an explicit illustration will be seen below.

Another issue on traps is their location: at surfaces or in the bulk. In fact, the surface traps behave similarly to the bulk traps,[22, 26] In the literature, the bulk traps are considered as a minor contribution to the OFETs' charge trapping[4, 21] since the bulk traps are believed difficult to be charged/discharged with sweeping the gate bias. It should be noted that, differing from the heavily doped silicon in which the band bending occurs only significantly near the silicon/dielectric interface, the traps in deep bulk obviously have a slight effect on the charge transport. However in organic transistors, the bulk traps may make a strong impact because all their extension from the OSC/dielectric interface till to the free surface could be filled. Therefore, if the open surface remains free without connection to a fixed potential (e.g. ground), the bulk traps might be a predominant limitation in organic transistors.

For the p-type OFETs, it is believed that the acceptor-like traps alter the on/off transition voltage and enhance the drain current, the donor-like traps, on the contrary, doesn't clearly move the on/off transition voltage but reduce the drain current.[21, 22] Here we employ the on/off transition voltage instead of the widely used threshold voltage because the threshold voltage loses its conventional meaning in organic thin-film transistors (OTFTs). Sometimes it is only a

fitting parameter, the enhancement/reduction of the drain current may change its fitting value.[27] Till now, there is one issue left on traps: the energy distribution.

B. Traps at a single energy level

This is the simplest distribution but a lot of works reported that it quite well accounted for their experimental data.[4, 21, 26] Fig. 4.11a shows the trap states at a single energy level (E_t). Such traps could be at the surfaces and/or in the bulk, either acceptor-like or donor-like.

Now a clear difference between surface and bulk traps arises: as increasing the applied gate bias, the bulk traps will be filled gradually but the surface traps will be filled up only once only if the trap density is moderate, as seen in the right illustration in Fig. 4.11a. For very deep surface traps, namely $\Delta E \approx E_G/2$, the traps at the two surfaces may have a comparable effect. If the traps are very close to the band edge, namely $\Delta E \approx 0$, the traps at free surface will have a minor effect due to the potential saturation. Such a trap-filling can be also applied to explain the often observed humps in the I-V and C-V characteristics around the threshold voltage,[4, 21, 25, 26] cf. Fig. 4.7. On the other hand, the bulk traps exhibit a consecutive impact.

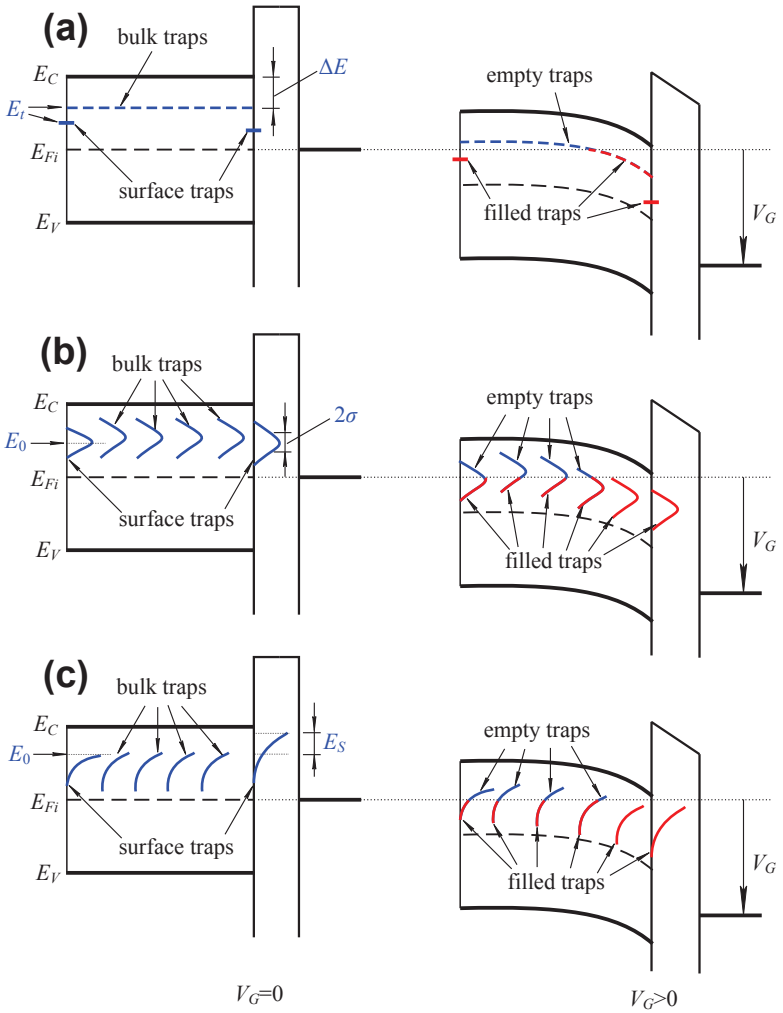


Figure 4.11 | Electronic traps in organic transistors with the density of states (DOS) at discrete energy levels (a), of Gaussian distribution (b) or of exponential distribution (c) in the bandgap. At V_G=0V, all traps are empty. At higher V_G, because of the entirely shifted bands of organic semiconductor, the Fermi level moves upward and the traps are correspondingly filled. Note that the traps at the free surface could also affect the overall charge trapping. The distributions of bulk traps that might differ from that of surface traps are assumed identical.

C. Traps with other energy distributions

If the impurity or defect density is much increased, the trap energies cannot be approximated to be at a single level but rather distributed in a large range. As shown in Fig. 4.11b, the DOS of trap states may reveal a Gaussian distribution with a mean energy (E_0) and a variance (σ^2). It can be represented by:[10]

$$N(E) = N_t \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-\frac{(E - E_0)^2}{2\sigma^2} \right] \tag{4.18}$$

where N_t is the volume trap density. The mean energy E_0 usually denotes the distribution peak and σ is the standard deviation. If the deviation σ is very small, all the trap states distribute around the peak of E_0 and thus behave similarly to the traps at a single energy level E_0.

Another popular DOS distribution is the exponential shape, as seen in Fig. 4.11c. This distribution is generally described by:[22]

$$N(E) = N_t \exp\left(-\frac{|E - E_0|}{E_S} \right) \tag{4.19}$$

where E_0 is the energy at which the maximum traps density appears, E_S is the characteristic width which denotes the DOS decay.

Note that in amorphous semiconductors, for instance polymer, there probably exists an extreme situation in which the DOS is a constant. It means that the bulk traps have a uniform density as a function of energy and behave like the interface states. In this study, the traps in all the depth of organic film are assumed to have a same distribution which might differ from that of surface traps.

4.1.5 FINITE ELEMENT SIMULATION INVOLVING TRAPS

The numerical simulations were carried out by using the finite element partial differential equation solver FlexPDE,[41] involving the surface and/or bulk traps. For the sake of simplicity, in this paper we analyze only the traps at a single level and with uniform DOS. The concentrations of the mobile charge and the trapped charge are treated similarly, for instance for acceptor-like bulk traps at a single level E_t, the concentration of free charges and trapped charges are:[4]

$$n(x) = N_C f(x) = \frac{N_C}{1 + \exp\left[\frac{E_G/2 - q\psi(x)}{kT} \right]} \tag{4.20}$$

$$n_t(x) = N_{At} f_t(x) = \frac{N_{At}}{1 + \exp\left[\frac{E_G/2 - \Delta E - q\psi(x)}{kT} \right]} \tag{4.21}$$

where N_{At} is the volume trap density, f_t is the trap occupation rate and here obeys the Fermi-Dirac statistics. If the traps reside at the surface, they could be calculated analogously as Eq.4.21 except that the location is at surfaces and the surface trap density N_{ST} is areal corresponding to:

$$N_{ST} = N_t \times t_{sc} \tag{4.22}$$

A, Interface states

We examined first the interface states, other traps are all kept to zero. By this way, we could analyze separately diverse charge trapping effects. Fig. 4.12 shows that the interface states at both surfaces exhibit similar influences. However, one can still recognize the stronger impact from the channel surface at high densities. This is because the band bending at this interface is larger than at open surface where fewer states are filled. When the states density is increased, the subthreshold slope (SS) becomes smaller, as expected.[25, 26]

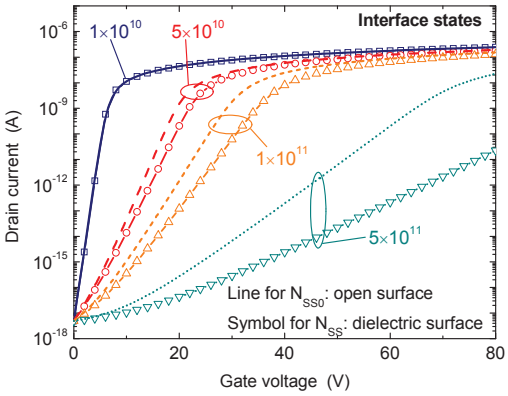


Figure 4.12 | Influence of the interface states ($1/eVcm^2$) on both sides of organic film, for a n-type transistor. At higher densities, the contribution from the channel surface displays a stronger influence.

B, Bulk traps at a single level

For the traps at a single level, we address the influence of trap density firstly, and then the energy level. In Fig. 4.13a, we can see that the drain current is severely affected by the trap density, in particular at N_{At} over $10^{17}/eVcm^3$, where the energy level is constant with ΔE=0.4eV. Note that the transfer characteristics curves at ΔE>0.4eV display a clear hump, as seen in Fig. 4.13b. The energy level is closer to the intrinsic Fermi level, the hump is more pronounced and the drain current in the subthreshold region is more trapping-limited. Such a result is expected since ΔE is greater the traps are easier to be filled while the Fermi level is moving upward.

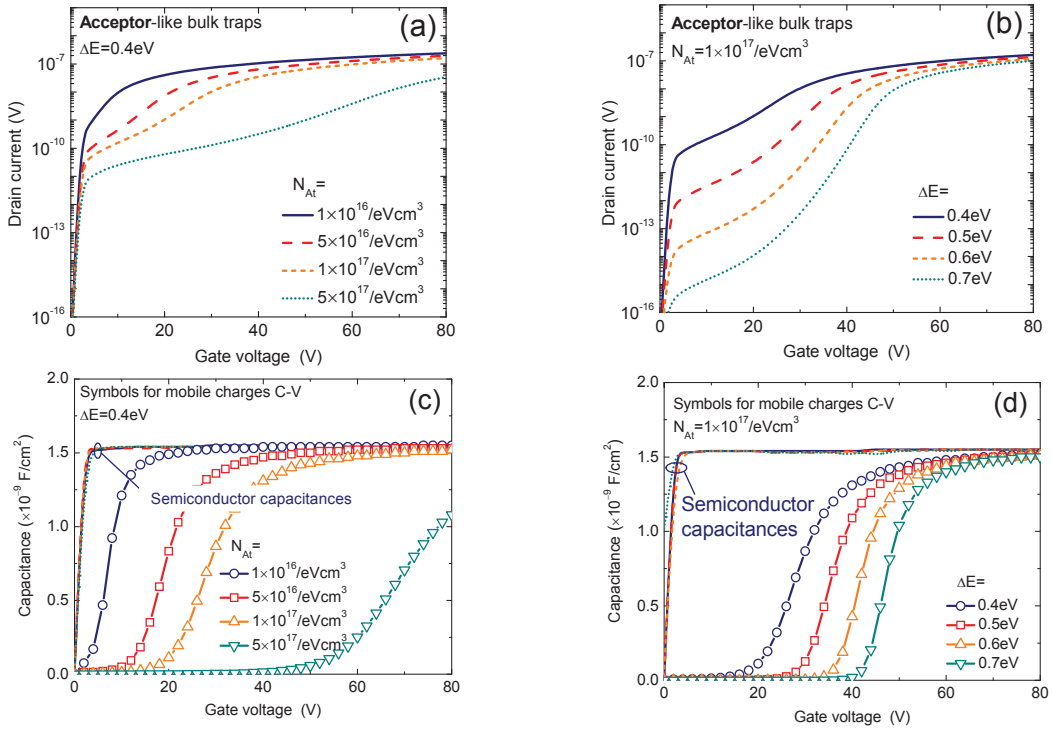
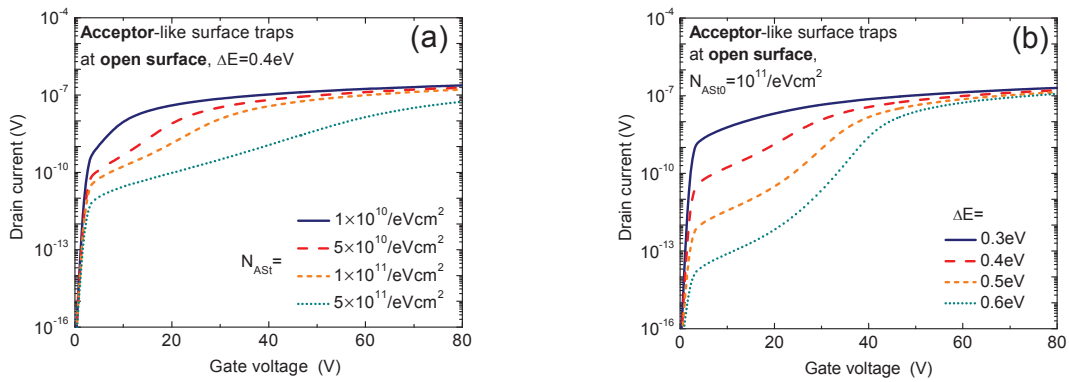


Figure 4.13 | Influence of the acceptor-like bulk traps on the drain current of a n-type transistor, for various trap density (a) and different energy levels (b), respectively. Note that a hump can be clearly identified when the trapping effect is strong enough. (c) and (d) show the influence of such traps on the C-V characteristics.



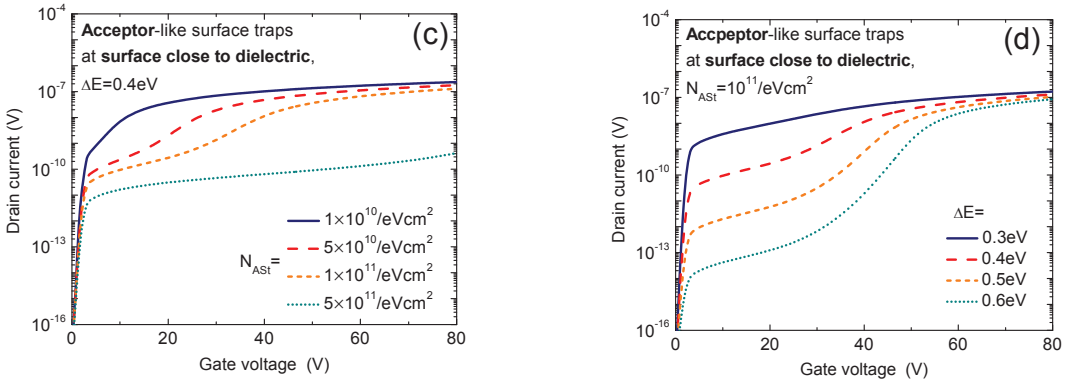
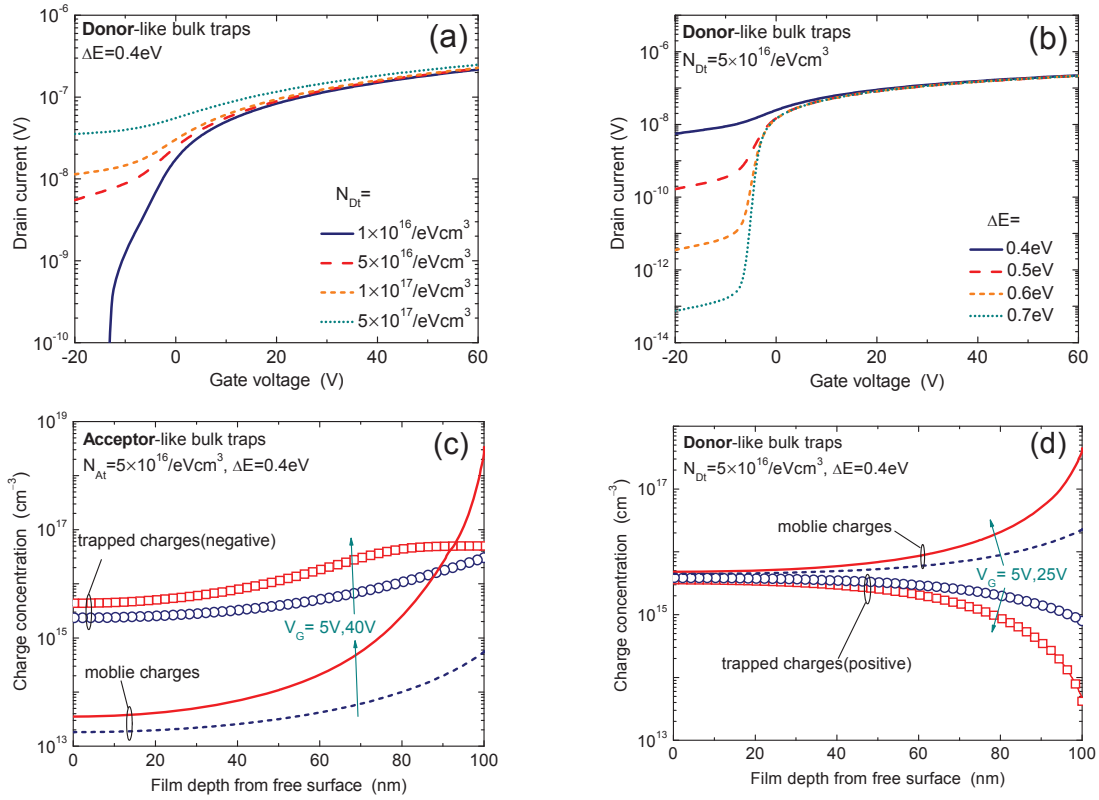


Figure 4.14 | The same process of Figures 13a and 13b applied to the traps at the open surface(a,b) and the dielectric surface (c,d). One can find the contribution from that of operating channel is more pronounced.

As discussed above, the trapped carriers, especially in the bulk, are difficultly released and cannot contribute to the current. The C-V analysis is thus carried out, as seen in Figs.4.13c and 4.13d. One can observe a slight change in the semiconductor C-V which represents the overall charge in the organic film. On the other hand, the mobile charge corresponding C-V strongly depends on the trap density and the energy level. The larger difference between the two C-Vs implies more trapped charge. Compared to the trap density, the energy level reveals an effect to shift the threshold voltage so that higher gate voltage should be applied to fill the traps extending into the entire bulk if ΔE is very close to $E_G/2$.

C, Surface traps at a single level

The surface traps were found behaving as the bulk traps.[26] Figs. 4.14a and 4.14b show the effect of various densities and various energies of the traps at free surface, respectively. Note that the traps at open surface have also an important effect on the carrier transport. If their density is sufficiently high and they are close enough to the intrinsic Fermi level, such traps may become a crucial limitation. Similarly in Figs. 4.14c and 4.14d, we analyzed the impact of the surface traps close to the dielectric. It was observed that they exhibit relatively stronger impact compared to those at free surface. Therefore, one could conclude that the surface traps and bulk traps have comparable effects if their distributions are not very different.



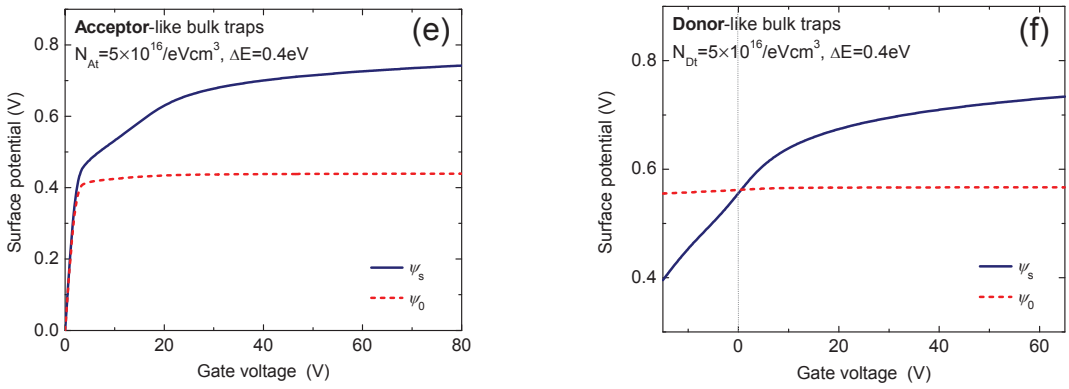


Figure 4.15 | Transfer characteristics in linear regime(V_D=0.2V) of an n-type OFET involving donor-like bulk traps at various densities(a) and at various energy levels(b). The current below threshold is significantly enhanced by traps, whereas the enhancement is slight above threshold. (c) and (d) show the charges distribution incorporating free charges and trapped charges by simulation for acceptor-like and donor-like bulk traps, respectively. The acceptor-like traps are fully filled near dielectric at high gate bias, on the other hand, the donor-like traps are compensated by the induced electrons. The ionized donor-like traps in the deep bulk improve the density of free charges and thus increase the current, particularly below threshold. (e) and (f) show the surface potentials for the simulations of (c) and (d), respectively. Here the flat-band voltage was given to be zero. The donor-like traps clearly shift the flat-band voltage and thus change the surface potentials.

D, Acceptor-like or donor-like traps at a single level

The previously analyzed traps are assumed to be acceptor-like for n-type transistors, the trapped charges read $Q_t=-qN_{At}f_t$. If the practical situation is opposite, the donor-like traps will be positively charged when not being filled by electrons, hence their charges become $Q_t=qN_{Dt}(1-f_t)$ with N_{Dt} being the donor-like trap density. Because of the similar behaviors between surface and bulk traps, here we focus only on the donor-like ***bulk*** traps which were seldom discussed before.[22, 26]

One can see that, compared to the acceptor-like traps, the donor-like traps give more positive charges $\Delta Q_t=qN_{Dt}$. Such additional positive charges causes a trend to shift the I-V characteristics toward negative values,[22] however the form of I-V curves is principally governed by the contribution of $-qN_{At}f_t$ which depends on the local potential. Meanwhile, the occupation rate $f_t\approx0$ at zero gate bias which means the traps are almost ionized or positively charged. This positive charge accumulates the electrons (at interfaces and in the bulk) and thus facilitates the free electron transport. The local potentials in the film at V_G=0V actually are not zero but rather have small positive values, that could be referred to as the flat-band voltages. Such behavior is in contrast with that for acceptor-like traps, since they are not ionized (or negatively charged) at $f_t\approx0$ and the current vanishes at zero V_G.[21]

In Fig. 4.15a one can see that, as increasing the density of donor-like traps, the drain current in the subthreshold region is increased, revealing a negative shift of on/off transition voltage. Fig. 4.15b shows the influence of energy level which doesn't affect the drain current above the threshold but reduces the subthreshold current. This is because the donor-like traps are farther away from the conduction band, the electron transport induced by this kind of traps is more difficult, e.g. by thermal activation. From another aspect, due to the non-zero potential at V_G=0V and the ionized traps,[26] farther away from the conduction band will result in fewer ionized charges, the enhancement of the drain current by such donor-like traps is less pronounced.

The distributions of free charges and trapped charges are also analyzed. In Fig. 4.15c, the acceptor-like bulk traps are gradually charged as more electrons are induced and hence, the trapped charge increases with V_G. In addition, the trapped charge density saturates in the layers close to dielectric and reaches the given trap density, implying the full filling of traps.[26] On the other hand, for donor-like bulk traps as seen in Fig. 4.15d, the V_G induced electrons compensate the positively charged (not filled) traps with filling the traps and hence the trapped charge density

decreases with V_G. Note that the density of free charge is significantly enhanced by the presence of donor-like traps, particularly in the deep bulk; the bulk conductivity is thus much improved.

Figs. 4.15e and 4.15f show the surface potentials for the above two simulations, respectively, where the flat-band voltage was supposed to be zero. For acceptor-like traps, the surface potentials are not significantly perturbed compared with the analytical results, cf. Fig. 4.6a. However for donor-like traps, the two surface potentials always exhibit positive values even at negative gate bias, and thus the transport below threshold is also significantly changed.

E, Bulk traps with uniform DOS

Finally, we studied the extreme case of uniform DOS. Because they behave like the interface states continuum, the conventional definition was applied, i.e. the upper half of the bandgap are acceptor-like traps and the lower half of the bandgap are donor-like traps. For n-type OFETs, the transfer characteristics taking account of such acceptor-like bulk traps are shown in Fig. 4.16, for various trap densities. One can readily observe the expected results.

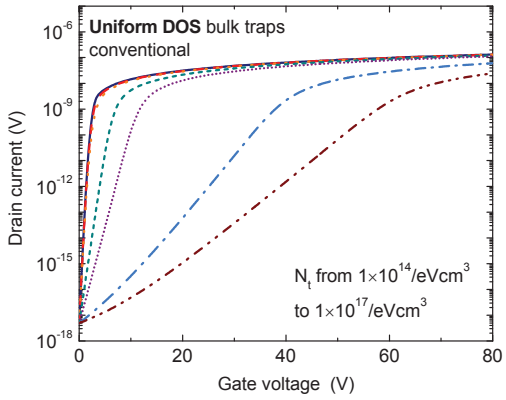


Figure 4.16 | Influence of traps with constant DOS on the transfer characteristics of the OFET. By using the conventional definition, the upper half of bandgap are acceptor-like traps and this kind of traps exhibit a similar influence as the interface states.

F, Fitting to the experimental data

Upon the above study, one tries to fit the simulation results to the experimental data. As shown in Fig. 4.17a, comparable good fittings are achieved by using the donor-like *bulk* traps and surface states. To distinguish them, we analyzed the C-V characteristics for the two cases, as shown in Figs. 4.17c and 4.17d. N_{ss} is same and the contribution to C-V is also the same, it is not a critical prerequisite here. A good agreement of the mobile charge C-V (DC C-V) is obtained since it represents the shape of transconductance and a good fitting of I-V certainly gives such a result. For bulk traps, the C-V of overall charge increases dramatically with V_G, whereas, for surface traps, this C-V exhibits a peak and after that follows the DC C-V. This is due to the fact that the gradually filled bulk traps continuously respond to C-V, differing from the one-time filled up surface traps. One cannot obtain good fitting for the I-V and C-V characteristics simultaneously with bulk/surface traps, but it is clear that such traps are not located at surfaces. Meanwhile one may notice the similar shapes of the overall charge C-Vs in the bulk traps simulation, a good agreement will be achieved if adding a shift. It implies that the trap density might be not constant at different film depth but rather be very small in the layers near the gate dielectric and increase closer to the free surface (with ΔE being constant). Increasing the gate bias, very few traps at first and afterwards more traps in deeper bulk are filled, leading to the observed C-V. Certainly, this inference may also change the I-V characteristics. However as discussed above, the bulk/surface traps exhibit similar influences on the drain current, i.e., the I-V characteristics are not sensitive to the location of traps if their densities and energy levels are not too different. We have tried to apply exponential or linear growth of trap density from the OSC/dielectric interface to deeper bulk, but a simultaneous good fitting of I-V and C-V characteristics is always unreachable. Nevertheless, one can still identify that the bulk traps are distributed in a narrow region close to the open surface, with a specific density profile. This is feasible since the well-known good quality of the TIPS-pentacene/Cytop™ interface is much better than the free surface, at which the TIPS-pentacene is directly deposited on the PEN substrate. Hence a large number of impurities and/or defects introduced from that surface might be responsible for the observed features in I-V and C-V characteristics. Meanwhile, our previous study showed the high quality of TIPS-pentacene film with large grains and high carrier mobility as well as low surface traps density.[42] The carrier mobility remains a constant value at liquid

helium temperature and next slightly increases as heating with a small activation energy of 2.3meV, the carrier transport is clearly not by hopping that is often observed in poor quality devices (e.g. amorphous and polycrystalline) and a hybrid of band-like and hopping transport is thus proposed. In other words, the main limitation on charge trapping in these TIPS-OFETs might be originated from the bulk traps close to the free surface. Another feasible way to distinguish surface/bulk traps could be to vary the organic film thickness since the bulk traps depend on the film thickness but the surface traps do not.

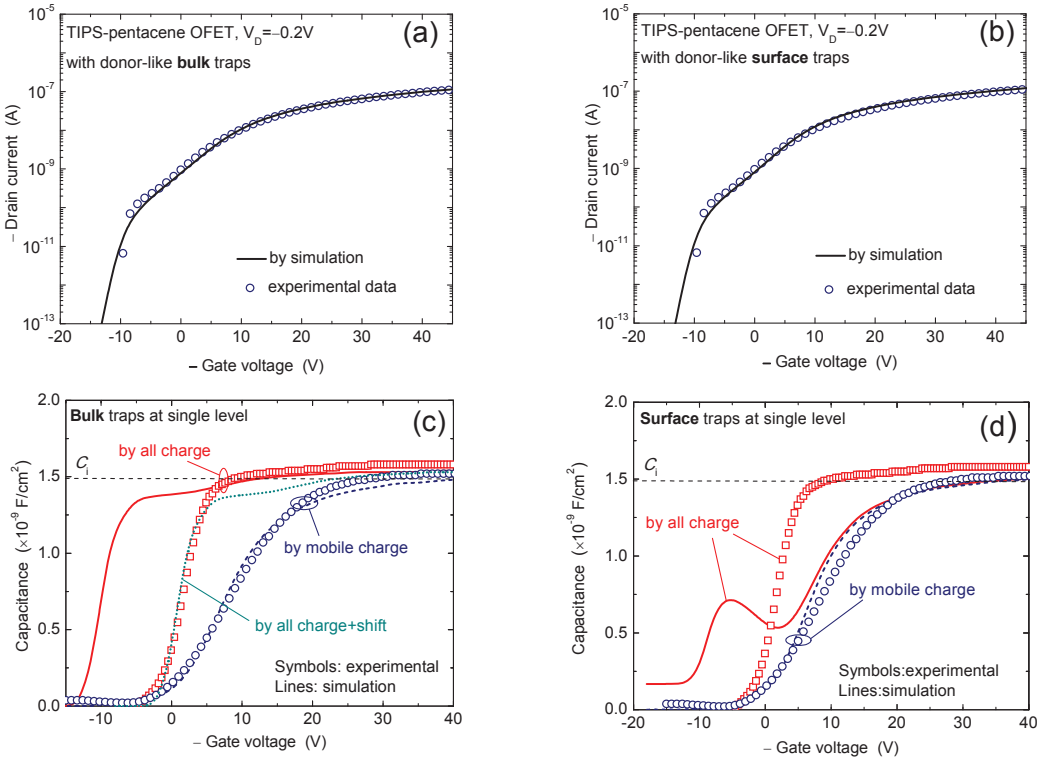


Figure 4.17 | Comparison of the simulation results with the experimental data, for that p-type TIPS-pentacene OFET. In figure (a), the donor-like bulk traps were applied, where N_{Dt}=1×10^{17}/eVcm^3, ΔE=0.41eV, N_{ss}=2×10^{10}/eVcm^2, N_{ss0}=0 and negative Q_{fix}=3.9×10^{-8} C/cm^2. In figure (b), the donor-like surface traps were applied, where N_{DSt}=3.9×10^{10}/eVcm^2, ΔE=0.38eV, N_{ss}=2×10^{10}/eVcm^2, N_{ss0}=0 and negative Q_{fix}=2.8×10^{-8} C/cm^2. (c) and (d) are the C-V characteristics of donor-like bulk and surface traps, respectively. Compared to the experimental result, the simulated semiconductor C-V of bulk traps gives too strong response, but the surface traps result in only a peak. The two extreme cases imply that the bulk and surface traps might coexist.

4.1.6 CONCLUSIONS

In summary, a modeling of the static electrical characteristics of organic transistors has been presented. Considering the intrinsic or lighted doped organic semiconductors and open-surface configuration in organic transistors, we proposed a 1-D analytical solution for Poisson's equation by which the potential profile and the carrier concentration in the organic film can be calculated for each gate voltage. It is found that the carrier transport in subthreshold region is a volume phenomenon rather than a superficial one because the surface potential at such a free surface is not fixed and the Fermi levels in the whole organic film vary nearly equally with gate bias. A quasi-superficial carrier accumulation only occurs at high gate biases. These features also explain the strong gate-voltage dependent contact resistance in staggered OFETs where the dominant contribution of bulk resistance is significantly modulated by the gate voltage.

A direct application to pentacene OFETs obtains good agreements with the experimental data but one met a deviation in subthreshold region while applying to TIPS-pentacene OFETs. After a detailed inspection of I-V and C-V characteristics one found that the deviation is due to the extrinsic influences of traps. The measured I-V characteristics correspond to only the mobile charge whereas the measured C-V data can respond to the overall charge, not only the mobile

charge but also the trapped charge. So there is a charge threshold difference between I-V and C-V characteristics and its value reflects the trapped charge. In consequence, we performed simulations on the basis of the analytical Poisson's equation solution with taking into account various types of traps. Because of the demonstration of free surface and volume subthreshold transport, the simulations highlight the importance of the traps at free surface and in the organic bulk (particularly their energy levels close to mid-gap), which have not attracted enough attentions in the community so far. Comparison of the simulation results and the experimental data indicated that the impurities and/or defects introduced from free surface into shallow bulk might be the reason for the observed special features in the I-V and C-V characteristics of our TIPS-pentacene OFETs.

The most important results of this paper are the demonstration of the impact of the open surface and the volume transport at small gate biases, which lead to several differences to the previous works. The results suggest that the treatments of open surface as well as the organic bulk are also important to improve the OFETs' performance.

4.2 CARRIER TRANSPORT MODELING (*based on the manuscript submitted to Journal of Applied Physics*)

Organic electronics nowadays is a fast emerging branch of microelectronics and it is further promoted by the growing demand for green energy and low pollution. Although considerable progress has been made in the past two decades, the understanding of carrier transport in organic semiconductors (OSCs) and in organic field-effect transistors (OFETs) is still limited.[43-45] It is believed that the weak van der Waals force interacting among molecules is responsible for narrow band width and lost of the conventional Bloch wave transport, which causes a different picture of carrier conduction in organic semiconductors from that in classical inorganic single-crystal bulk, such as silicon. In addition, the commonly existing defects and the relatively strong lattice vibration give rise to an evident transport mechanism by hopping.[16] To identify the transport process, carrier mobility at variable temperatures[23] and various gate voltages/carrier densities[12, 46] are widely applied. The measured macroscopic mobility (μ) dependences on temperature (T) indeed reflect the microscopic carrier transport, e.g., negative $d\mu/dT$ for band-like transport in delocalized states and positive $d\mu/dT$ for thermally activated hopping in localized states.[45] Similarly for the gate voltage(V_G) dependences, one has negative $d\mu/dV_G$ for band-like transport and positive $d\mu/dV_G$ for hopping.[46] Meanwhile one can see that, the consecutive amelioration of material engineering and fabrication technology significantly reduce the extrinsic influences (e.g. structural defects) and improve the deposited film quality (e.g. molecular organization),[16] the observed performances continuously approach to their intrinsic characteristics. For instance, the band-like transport with high mobility has been reported in single-crystal rubrene, by Hall Effect measurements.[47, 48]

As compared to organic bulk semiconductors, the carrier transport is much more complex in organic transistors where very high density of carriers are confined in a narrow channel at high gate biases, the interface quality and the gate dielectric may play an important role there.[49, 50] Moreover, the transport in contact region even more complicates this issue.[17, 51-53] By means of Hall Effect measurements, the band-like transport in the OFETs with polycrystalline pentacene[54] or single-crystal rubrene[55] have also been observed. However, an indication of band-like transport in OFETs from conventional current-voltage (I-V) characteristics is rarely reported.[56, 57] This is because a number of additional effects on OFETs' mobility need to be addressed, such as contact influence,[58] gate-voltage[12] and drain-voltage dependences.[59] In addition, the lack of a universal and stable extraction method for mobility increases the difficulty, particularly at low temperatures for short-channel devices.

Recently, we measured a set of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) OFETs. These transistors are fabricated on the basis of a plastic PEN substrate (cf. Fig. 4.18a) covering with patterned gold contacts, the TIPS-pentacene, dielectric (Cytop^{TM}) and gate electrode (based on silver ink) are subsequently gravure printed, forming the top-gate (TG) and bottom-contact (BC) geometry as seen in Fig. 4.18b. With delicately controlling the preparation conditions, large grains are obtained, as shown in Fig. 4.18c. They show remarkable performance, a mobility as high as 6 $cm^2V^{-1}s^{-1}$ is measured at room temperature (cf. Figs. 4.18d,e) with moderate contact resistance $R_C \approx 10^3$ Ωcm and $I_{on}/I_{off} \approx 10^5$. The surface trap density obtained by low-frequency noise measurements[60] is found to be strikingly around 10^9-10^{10} $eV^{-1}cm^{-2}$, comparable to that in classical silicon MOSFETs.[34] Their high reliability guarantees the low temperature measurement down to liquid helium temperature against any damage and abnormality, particularly in the linear regime of output characteristics, enabling an insight into the intrinsic carrier transport mechanism in TIPS-pentacene, a promising material for current organic electronics. At the same time, the mobility shows a thermal activation at intermediate temperatures but the corresponding activation energy (E_a) is as small as 2.3meV, similar to that observed in single-grain pentacene OFETs by Minari *et al.*[61] Moreover, the mobility doesn't vary monotonically with E_a but rather remains a constant value at low and high T. This temperature independent mobility at low T has already been reported by Horowitz *et al.*,[12, 61] and it was attributed to the tunnel transfer through grain boundaries. A temperature independent mobility over large temperature range was also found in high quality pentacene OFETs by Nelson *et al.*,[58] and it was excluded from the thermally activated hopping as a fundamental transport mechanism. All these results motivate a thorough study on the carrier transport by OFETs' mobility.

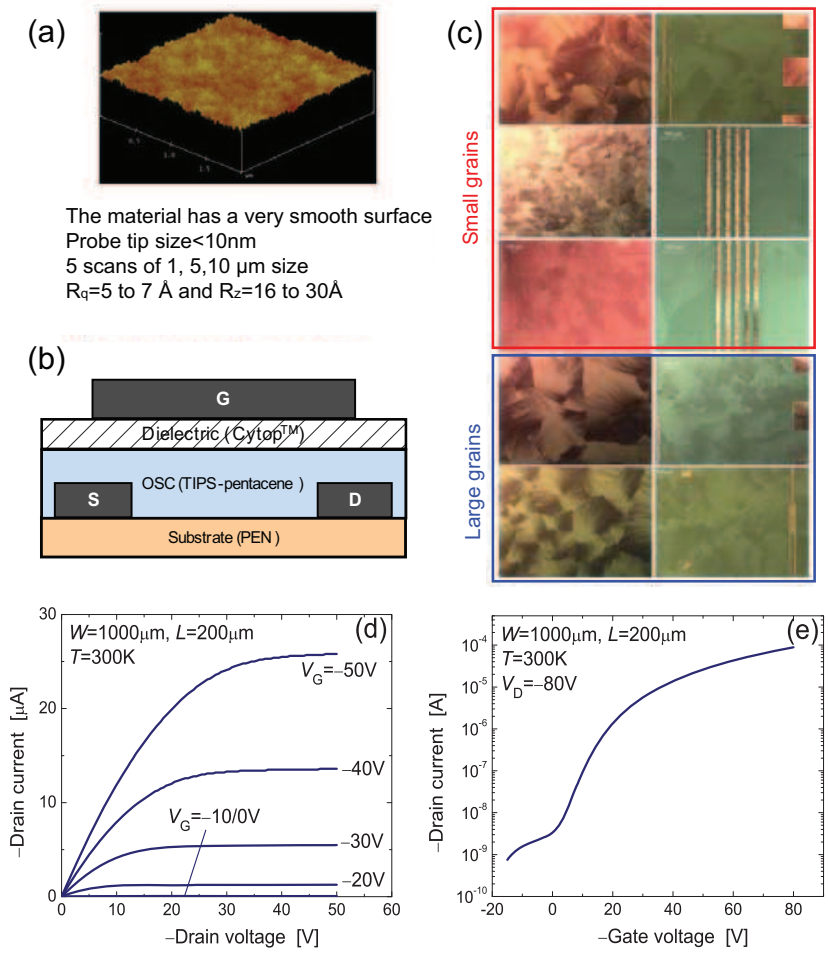


Figure 4.18 | (a) Microscopic image of the treated surface of PEN substrate. (b) Schematic illustration of the OFETs' configuration. (c) Morphology of TIPS-pentacene, the upper six microscopic images show poor quality and thus small grains are formed. The lower four microscopic images show good quality and large grains are obtained. (e) and (f) are the output and transfer(saturation regime) characteristics of a highest mobility(≈6 $cm^2V^{-1}s^{-1}$) OFET.

Upon these considerations, in this paper we firstly report on the temperature dependence of mobility in our TIPS-pentacene OFETs based on normal I-V characterizations. To account for the observed temperature dependences of mobility that have never been reported so far, a transport analysis in non-crystal system is subsequently proposed, with using the Kubo-Greenwood integral by which one can address the effects of microscopic transport in the band on the macroscopic carrier mobility. Finally, the gate-voltage or carrier density dependences of mobility are analyzed. The novelty of this work relies on the fact that the mobilities extracted by various methods are studied with respect to channel length, gate and drain voltages, highlighting the importance of mobility extraction and the severe contact effect for transport study. The mobility modeling enables us to better understand theoretically the origins of the carrier transport in such organic transistors.

4.2.1. Mobility measurements

A, Saturation field-effect mobility

First, the transfer characteristics in saturation regime (drain voltage V_D=−60V) at various temperatures T are shown in Figs. 4.19a,b, for two OFETs of channel length L=5μm and L=100μm, respectively. A saturation field-effect mobility μ_{fe} is commonly evaluated from the slope of the square root of the drain current against the gate voltage $I_{Dsat}^{0.5}(V_G)$, as seen in the same figures. For short-channel OFET, a good linearity is not attained even at very high gate voltage, especially at low T.[56, 62] Such a problem is not completely alleviated in longer-channel transistors. Therefore, this non-linearity might be due to the drain-voltage and/or gate-voltage dependent mobility, and this impact is more pronounced in short-L transistors.[12, 59] In Figs. 4.19c,d, despite very different μ_{fe} in both OFETs a similar variation is still identified: nearly constant at low T and afterwards, increases at intermediate T and finally saturates at high T.

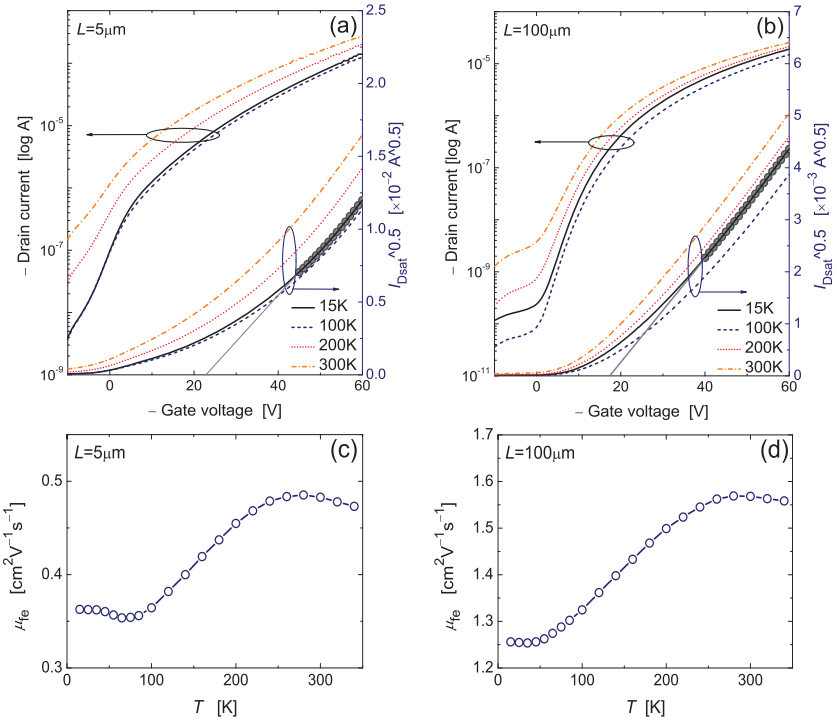


Figure 4.19 | (a) and (b) Transfer characteristics in saturation regime at V_D=−60V and the square root of drain current, for two OFETs L=5μm(W=2000μm) and L=100μm(W=1000μm), respectively. A few temperatures are selected for illustration. (c) and (d) are the evaluated field-effect mobility by the slope of selected data region seen in (a) and (b).

B, Low-field mobility

Next, we apply an alternative method to extract the mobility. In linear regime (V_D=−0.5V), the transconductance $g_m(V_G)=\partial I_D/\partial V_G$ is shown in Figs. 4.20a,b. The low-field mobility μ_0 is evaluated from the slope of Y function $Y(V_G)=I_D/g_m^{0.5}$,[30] as shown in Figs. 4.20c,d. This mobility

was proved more intrinsic than the effective mobility and the saturation field-effect mobility, in particular free from the contact resistance influence. As compared to the above non-linear $I_{D\text{-}sat}^{0.5}(V_G)$, Y function is always a straight line even in short-L OFET and at T=15K. The mobility and the threshold voltage thus can be more safely evaluated. Comparing the previous μ_{fe} in Figs. 4.20e,f, a large difference in short-L OFET arises. Only from extraction aspect, μ_0 is clearly more reliable than μ_{fe}.

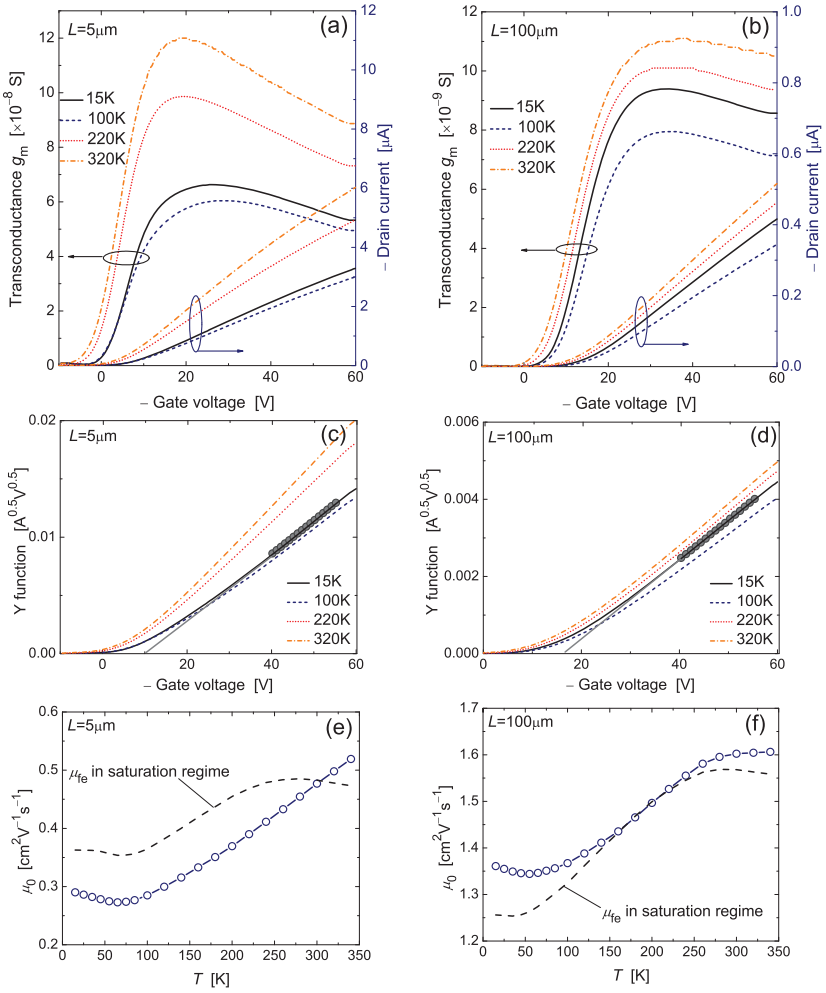


Figure 4.20 | (a) and (b) Transfer characteristics in linear regime (V_D=–0.5V) and transconductance, for the two OFETs, respectively. (c) and (d) are the Y functions for mobility and threshold voltage extraction. Good linearity can be always observed even in the short-L OFET ant at T=15K. (e) and (f) are the extracted mobility, where the symbols indicate the low-field mobility extracted by Y function, and the dashed lines represent the previously obtained saturation field-effect mobility.

C, Effective mobility

For further verification, another mobility extraction method by output conductance is applied. This method allows us to investigate the mobility dependences on drain and gate voltage. The output characteristics at a fixed V_G=−50V are shown in Figs. 4.21a,b. With the output conductance $g_D=\partial I_D/\partial V_D$ (cf. Fig. 4.21c,d), an effective mobility can be derived as $\mu_{eff}=g_D L/[WC_i(V_G-V_T-V_D)]$ in linear regime and at strong accumulation, where W is the channel width, C_i is the unit area capacitance of gate dielectric and V_T is the threshold voltage. It should be mentioned that the V_T values extracted by Y function are preferred here because their better linearity reflects more reliable charge threshold. Figs. 4.21e,f show the contact resistance corrected μ_{eff},[30] and it can be seen that larger improvement and higher sensitivity to V_D are found in shorter-L OFET, as expected.[63] Moreover, the data of L=5μm exhibits a peak at first and then declines with V_D, whereas such a peak is not obvious in longer-L OFET. Note that we didn't observe the super-linearity and the lost of current saturation in output characteristics that was recently reported by Sakanoue *et al.* in short-L TIPS-pentacene OFETs at low T, at high gate and drain voltages.[56] Such behaviors should also result in a peak in output conductance and thus in mobility versus V_D at small drain voltages, but with a mobility starting to increase from zero. This feature is very

similar to the drastically increased contact resistance at liquid helium temperature, in the lightly doped drain (LDD) silicon MOSFETs.[64] It was interpreted by the impurity freeze-out at ultra low *T*, leading to a complete deactivation of the device channel. Increasing the drain and gate voltage, the electric field assists the impurity ionization and the channel recovers. Certainly, one cannot directly apply it to organic transistors but a close similarity concerning the charge injection in staggered structure could be still recognized.

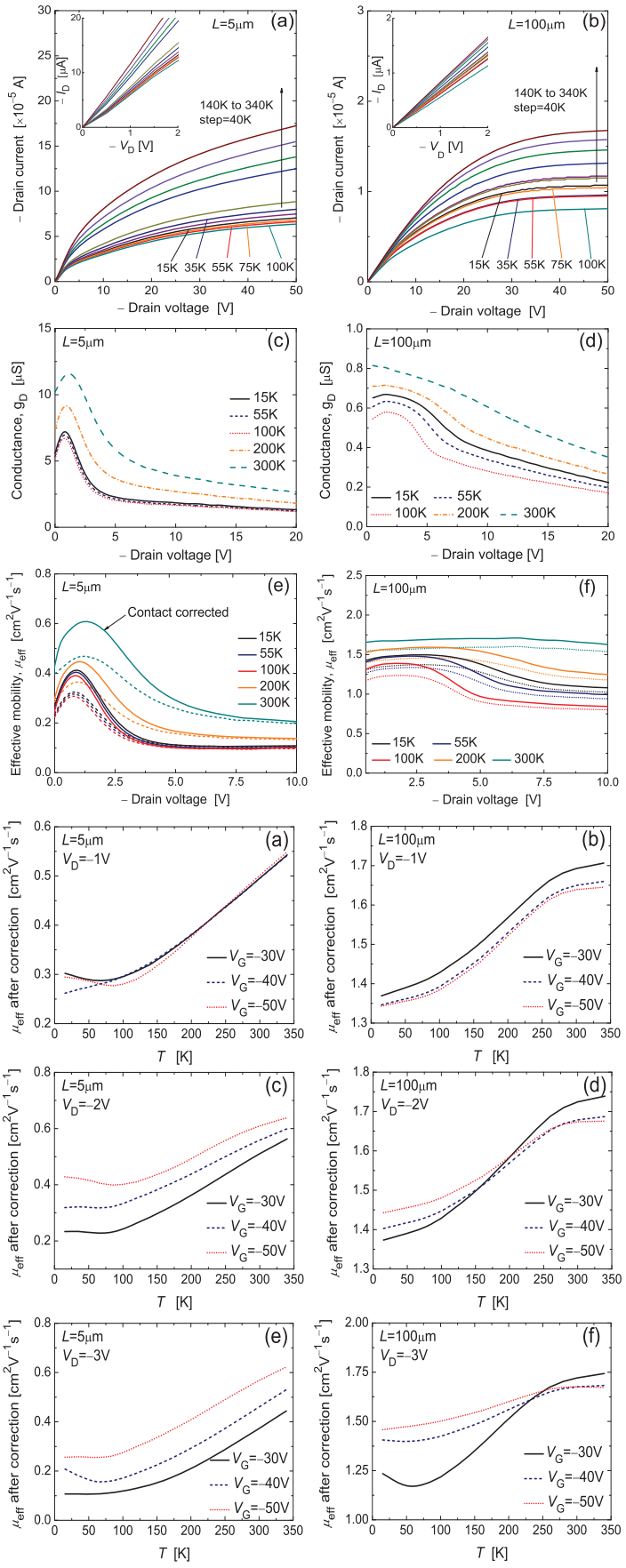


Figure 4.21 | (a) and (b) Output characteristics at V_G=–50V and various temperatures, for the two OFETs, respectively. The insets indicate the linear region at small drain voltages. Nonlinearity cannot be clearly seen even in the short-*L* transistor and at low *T*. (c) and (d) Output conductance at various temperatures. (e) and (f) Derived effective mobility, where the solid lines represent the contact resistance corrected mobility and the dotted lines represent the uncorrected one.

Figure 4.22 | Contact corrected effective mobility at various gate voltages and various drain voltages.

The same process is applied to two more V_G=−40V and −30V, chosen not too small in order to ensure the V_D variation for mobility evaluation. As shown in Figs. 4.22, V_G doesn't clearly alter $\mu_{eff}(T)$ in short-L OFET (but V_G increases mobility at higher V_D, cf. Figs. 4.22c,e), a somewhat opposite trend is found in the longer-L transistor, cf. Figs. 4.22b,d,f. However, it is in agreement with the band-like transport by which higher gate field increases phonon scattering and surface roughness impact and thus, the effective mobility decreases with gate voltage. This result implies the different transport in short/long-L devices. In any case, the set of curves are almost parallel at different T, which means that the drain/gate voltage shifts the mobility value but does not change its temperature dependence.

D, Discussions on mobility results

The three studied mobilities are summarized in Figs. 4.23a,b. It is clear that μ_0 and μ_{eff} are very close, whereas μ_{fe} differs slightly. More importantly, the temperature dependence of μ_{fe} is substantially changed in short-L OFET, which is indeed related to the extraction method. Considering ease of use, the μ_0 is selected for the next analysis and one will readily see a different picture at high T in the two short/long-L transistors.

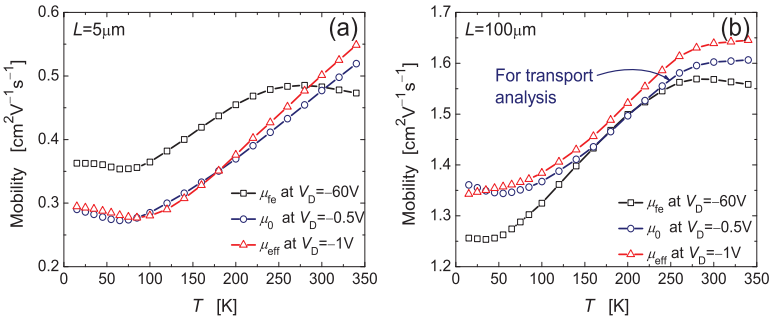


Figure 4.23 | (a) and (b) Three mobilities obtained by different method: μ_{fe} (by $I_{Dsat}^{0.5}(V_G)$), μ_0 (by Y function), μ_{eff} (by output conductance with contact resistance correction).

In consequence, the μ_0 in several OFETs of various channel lengths are examined, cf. Fig. 4.24a. Note that the mobility level increases significantly with channel length except for L=100μm and moreover, stronger temperature dependence is found in shorter-L devices.[58]

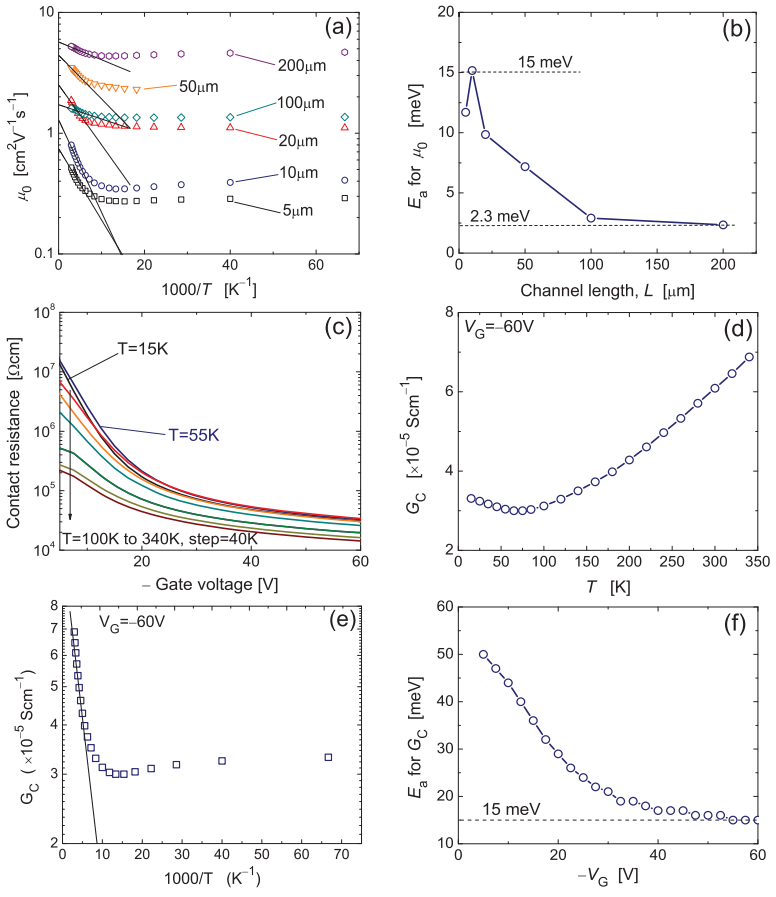


Figure 4.24 | (a) Arrhenius plots for the low-field mobility extracted in six transistors of different channel length. (b) Activation energy extracted in (a). (c) Contact resistance obtained by modified TLM, for six transistors of various channel lengths. (d) Average contact conductance for the set of transistors at V_G=−60V, for each measured temperatures. (e) Arrhenius plot for the average contact conductance at V_G=−60V. Activation energy can be obtained at high temperatures. (f) Activation energy of contact conductance obtained at various gate voltages.

These results could imply a contact limitation on the overall transport. An activation energy E_a extracted at intermediate temperatures is plotted versus channel length, as shown in Fig. 4.24b. Interestingly, the E_a decreases with L and stabilizes at E_a≈2.3meV in long L. This small E_a and non-zero mobility at low temperature indicate that the transport mechanism is not the conventional thermally activated hopping as $\mu_0=\mu_{00}\exp(-E_a/kT)$, where μ_{00} is a specific mobility, k is the Boltzmman constant and E_a characterizes the energy difference between the band edge and the trap states that generally distribute in the bandgap at dozens of meV from the band edge.[23] That characteristic E_a should be much greater than our E_a≈2.3meV. Furthermore, the thermal activation vanishes at low temperature and the mobility remains a nearly constant value,[12, 61] which would not be the case for fully activated hopping transport.

Note also the large E_a=15meV in Fig. 4.24b for short L, which might imply contact dominated transport, so we perform the contact resistance extraction using the modified transfer-line method (TLM)[65] at each T. Here we focus on the contact conductance $G_C=1/R_C$ (R_C cf. Fig. 4.24c). In Fig. 4.24d, $G_C(T)$ seems to vary similarly as that of $\mu_0(T)$ in short-L devices, implying the same transport process. The E_a is evaluated (cf. Fig. 4.24e) and a smaller value is obtained at higher V_G, consistent with the filling of deep traps in the relatively more disordered contact region (BC contacts) by sweeping the Fermi level towards the band.[46, 66, 67] However the E_a variation is not big enough to form a crossing point that is predicted by Meyer-Neldel rule, often observed in the transport in disordered media.[63] In Fig. 4.24f, one should notice the stabilized E_a=15meV that was discussed for the μ_0 activation in short-L transistors. One can conclude now that the overall carrier transport in short-L OFETs is dominated by contact proximity and a more intrinsic transport analysis would be better undertaken in long-L transistors. Hence the small E_a=2.3meV reflects the channel transport and E_a=15meV reflects more the contact region transport. As seen in Fig. 4.23b, the μ_0 in the OFET of L=100μm is chosen for the transport analysis.

4.2.2 Mobility modeling with Kubo-Greenwood integral

Up to now, several transport models have been proposed,[12, 46, 68, 69] here we provide some discussions of our observations. Following ref.,[70, 71] we suppose a Gaussian distribution for the band density of states (DOS) $N(E)$ as it well accounts for the OSCs characteristics,[70, 72, 73]:

$$N(E)=\frac{N_t}{\sqrt{2\pi}\Delta E}\exp\left[-\frac{(E-E_0)^2}{2\Delta E^2}\right] \tag{4.23}$$

where N_t is the characteristic band DOS (here fixed at 2×10^{21}cm^{-3} for TIPS-pentacene), ΔE is the standard deviation and E_0 is the band center energy (assumed to be zero as a reference). Because the band width in most of OSCs is very narrow (≈0.1eV), ΔE is chosen in the range of 0.05eV-0.2eV. Note that ΔE here doesn't mean the effective bandwidth alike in the classical inorganic semiconductors because the total band states remain the same, hence larger ΔE represents a broader distribution due to disorder,[70] for instance the BC contact region in our case.

The conductivity σ is calculated by using the Kubo-Greenwood integral:[74]

$$\sigma_{total}(E_F,T)=\int_{-\infty}^{+\infty}\sigma(E)\left(-\frac{\partial f}{\partial E}\right)dE \tag{4.24}$$

where σ is the conductivity, $f(E,E_F,T)$ is the Fermi-Dirac distribution, E and E_F are the energy and the Fermi energy, respectively. The macroscopic conductivity σ_{total} can be calculated by the microscopic energy-dependent ones $\sigma(E)$ in the band, which is given by:[74, 75]

$$\sigma(E)=q^2N(E)D(E) \tag{4.25}$$

where q is the electron charge, $N(E)$ is the distribution of density of states (DOS) in the band and $D(E)$ is the diffusivity for each energy. Having calculated $\sigma(T)$, the effective mobility μ_{eff} can be obtained as:

$$\mu_{eff}(E_F,T)=\frac{\sigma_{total}(E_F,T)}{qN_{total}(E_F,T)} \tag{4.26}$$

where N_{total} is the total carrier concentration as:

$$N_{total}(E_F,T)=\int_{-\infty}^{+\infty}N(E)f(E,E_F,T)dE \tag{4.27}$$

The μ_{eff} here is calculated from the OSC conductivity and charge concentration, and it represents the apparent or average mobility for overall carriers in the OSC bulk. This μ_{eff} for OSC should be equal to the intrinsic carrier mobility in OFETs, which is the low-field mobility μ_0 previously extracted by Y function. Now one can find that if the condition parameters (i.e., E_F and T) are fixed, the distribution of $D(E)$ will be the major factor to determine μ_{eff}. So, we discuss three possible $D(E)$ and the resulting effects on μ_{eff}.

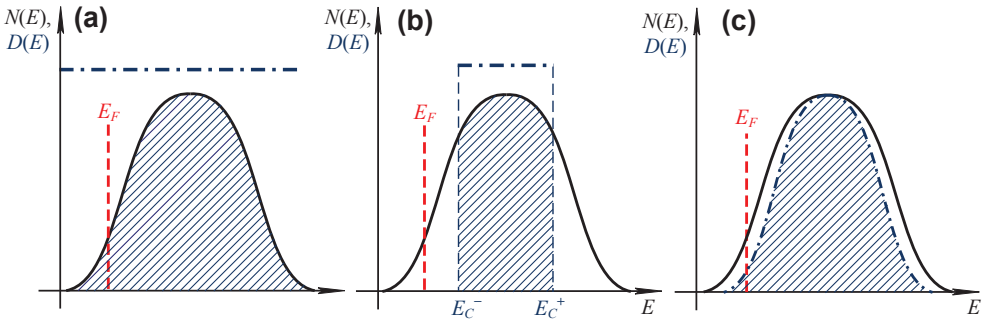


Figure 4.25 | Band structure in organic semiconductor, where the Gaussian curve (solid line) represents the density of states. The dash dot line represents the diffusivity $D(E)$, with constant(a) and window(b) and Gaussian(c) distribution in energy.

A, Constant $D(E)$ with fully band-like transport

If the diffusivity is constant in the band as shown in Fig. 4.25a, all elementary energies will equally contribute to the band conductivity. This constant $D(E)$ corresponds to bank-like transport in a band with non localized states, and it will give a high mobility which declines with T following $\sim T^{-1}$, for not too low temperature and not too high carrier density, as seen in Fig. 4.26a. This is a characteristic of a Maxwell-Boltzmann statistics governed by the Einstein relation $\mu=qD/kT$.[70, 76] According to the Maxwell-Boltzmann statistics, when the carrier density is not very high (i.e., E_F is relatively low, thus leading to $\exp[(E-E_F)/kT]>>1$) the Fermi-Dirac distribution in Eqs. 4.24 and 4.27 can be approximated as:

$$f(E,E_F,T)\approx\exp\left[\frac{-(E-E_F)}{kT}\right] \tag{4.28}$$

If the diffusivity is constant (denoted by D) in the band, Eq. 4.25 will read:

$$\sigma(E)=q^2N(E)\times D \tag{4.29}$$

Thus the total conductivity in the band by using the Kubo-Greenwood integral (at not too low T) will become:

$$\sigma_{total}(E_F,T)=\frac{q^2D}{kT}\int_{-\infty}^{+\infty}N(E)\exp\left[\frac{-(E-E_F)}{kT}\right]dE \tag{4.30}$$

Note that the total carrier concentration is equal to the term on the right side of Eq. 4.30 and reads:

$$N_{total}(E_F,T)=\int_{-\infty}^{+\infty}N(E)\exp\left[\frac{-(E-E_F)}{kT}\right]dE \tag{4.31}$$

Therefore, the effective mobility is obtained as:

$$\mu_{eff}(E_F,T)=\frac{\sigma_{total}(E_F,T)}{qN_{total}(E_F,T)}=\frac{q}{kT}\times D \tag{4.32}$$

One will find that Eq. 4.32 is exactly the Einstein relation. Increasing the temperature T, μ_{eff} will decline with T following $\sim T^{-1}$. Such a constant $D(E)$ reflects perfect crystal structure without

defects, and it should mainly apply to high quality OSCs, e.g. single-crystal,[44, 47, 48] consistent with the inherent band-like carrier transport in delocalized states over large temperature range.[57]

B, Window $D(E)$ with localized states band tails

Compared to the above ideal case, a large number of disorder-induced extrinsic defects are often distributed in OFETs and the localized states need to be taken into account. As shown in Fig. 4.25b, two borders (E_C^- and E_C^+) symmetrically divide the band into two parts: the delocalized states core and the localized states tails. The diffusivity is constant within the core but becomes zero outside, this is because the carriers move freely in the extended states with high mobility but in the localized states tails, the carriers can transport only by hopping whose rates are enhanced by phonon vibration and thereby, the observed mobility is very small (generally less than $1 cm^2V^{-1}s^{-1}$) and exhibits a thermal activation behavior. The two borders act as mobility edges.[75]

This kind of $D(E)$ will give rise to a dominant hopping transport when the carrier density is not very high relative to that of the localized states, i.e., $E_F<E_C^-$. At low temperatures, almost all carriers lie in the localized-states tail and the thermal activation is negligible, the carriers are completely localized. As a result, μ_{eff} falls down to zero at low T. Increasing T, the carriers obtain energy from phonons and hop more efficiently, manifesting a thermally activated mobility, as seen in Fig. 4.26b. This case is often observed in amorphous polymer and polycrystalline OFETs where a large number of defects exist and the transport is nearly accomplished by hopping.[23]

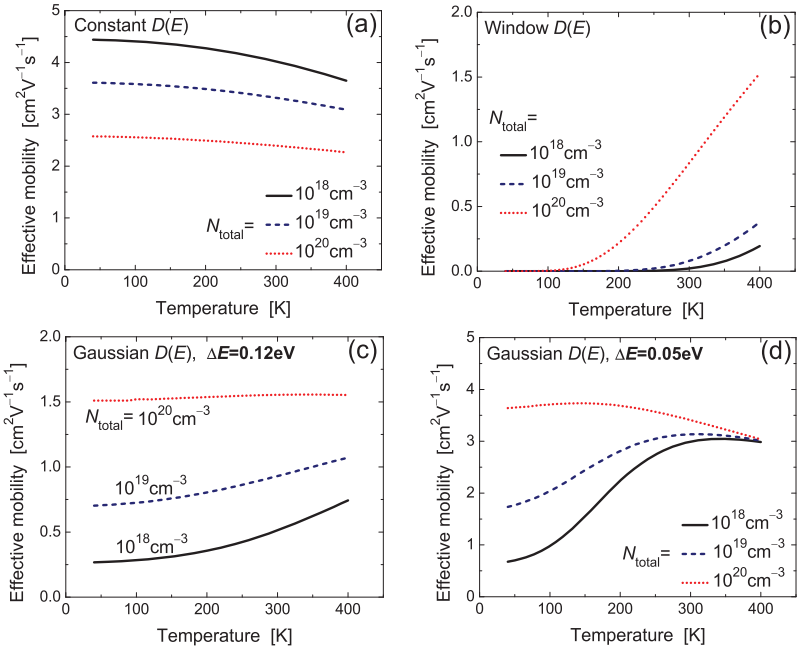


Figure 4.26 | The calculated effective mobility at various carrier densities (N_{total}), for the three $D(E)$ shown in Fig. 7, respectively. Here the total band density of states (N_t) is $2\times10^{21}cm^{-3}$, ΔE=0.1eV. For (b), E_C^-=–0.1eV, the three carrier density (10^{18}, 10^{19} and $10^{20}cm^{-3}$) correspond to E_F=–0.43eV, –0.33eV and –0.21eV at T=300K, respectively, i.e., $E_F<E_C^-$. For the Gaussian $D(E)$ in (c, d), the standard deviation is $0.8\Delta E$.

C, Gaussian-like $D(E)$ with gradually degraded delocalized-localized states hybridization

Even though the two previous situations are abundantly reported in the literature, sometimes they cannot interpret experimental results, e.g. constant non-zero mobility at low T,[12, 61] small activation energy and even constant mobility over large temperature range.[58, 61] So, a more generic description is required. In Fig. 4.25c, the diffusivity is degraded from band center to tails, the transport also gradually deviates from pure band-like, probably due to the existence of a small quantity of localized states and in particular at the band edges. For simplicity, a Gaussian-like $D(E)$ with a smaller ΔE compared to that of the DOS is assumed here.

As seen in Figs. 4.26c,d, the calculated $\mu_{eff}(T)$ does exhibit the similar variation as observed, implying that this Gaussian-like distribution of $D(E)$ is able to explain our results. The ΔE=0.12eV and 0.05eV correspond to the case of our short-channel and long-channel devices, respectively. For better illustration, Fig. 4.27 shows the details of the carrier distribution and the

conductivity in the band as well as the Fermi level at various temperatures, for the two different ΔE cases. **i)** At low T, due to the degenerate statistics and according to the Kubo-Greenwood integral, the band conductivity $\sigma_{total}(T)$ reduces to the element at Fermi energy, i.e. $\sigma(E_F)$, as seen in Figs. 4.27c, d. This single-energy contribution is independent of temperature, resulting in a constant mobility at low T. If the carrier density remains constant (N_{total}=10^{19}cm^{-3} here), the corresponding E_F is lower in more disordered system, the smaller $\sigma(E_F)$ thus gives a smaller constant mobility, cf. Figs. 4.26c, d.[12, 70] **ii)** Increasing T, more carriers distribute at higher energies where the diffusivity is higher, as shown in Figs. 4.27a,b. At the same time, the term of $\sigma(E_F)(-\partial f/\partial E)$ in the Kubo-Greenwood integral is no longer confined in a small energy range. The two contributions simultaneously increase mobility with heating. This improvement is more pronounced in larger ΔE system since the Fermi level locates closer to the band tails, in agreement with stronger thermal activation in poorer quality devices.[58] It should be noted that such a progressive increase for $\mu(T)$ cannot justify the fully hopping transport by which a E_a of dozens of meV is often deduced.[23] **iii)** Increasing T further, such two extensions spread out over the whole band and become saturated first in smaller ΔE system. Meanwhile, the Fermi level decreases with T, greater in smaller ΔE system. In consequence, the mobility tends to saturate and even decrease with T in the ordered system (smaller ΔE),[58, 61] however in larger ΔE case, the non-terminated extensions and the slighter decline in E_F give a continued increase of mobility, in agreement with the contact dominated transport in short-L transistors. This generic Gaussian $D(E)$ is applied for the following analysis.

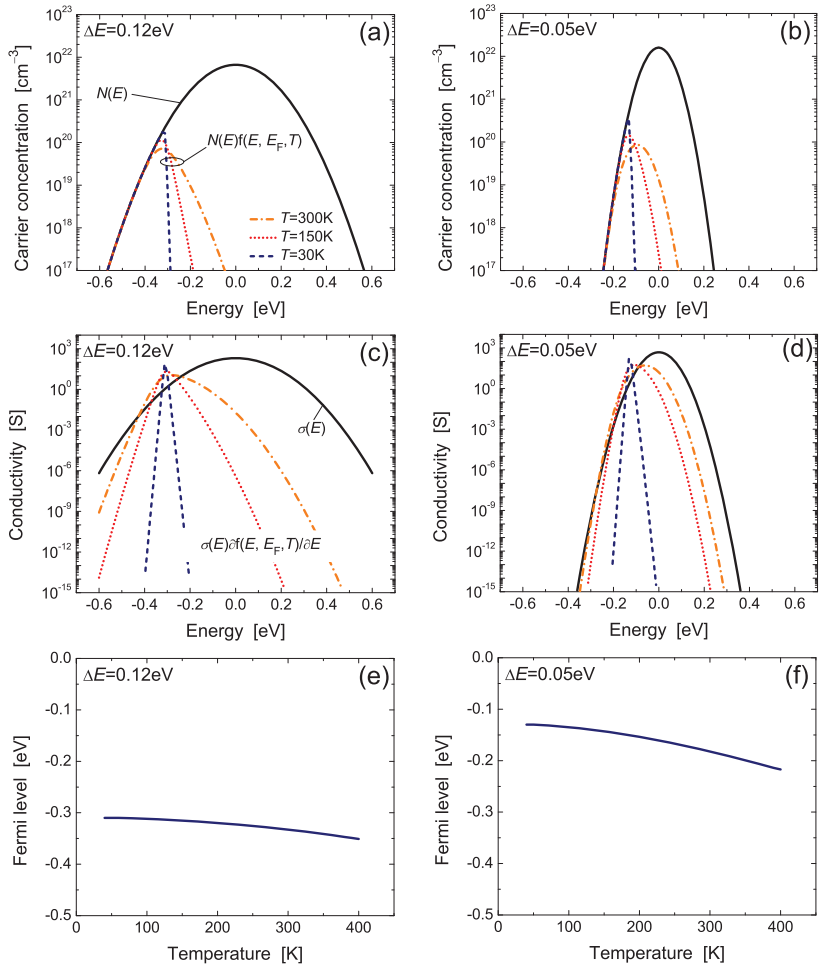


Figure 4.27 | (a) and (b) are the carrier distribution in energy with respect to the DOS at a constant carrier density N_{total}=10^{19}cm^{-3} since this N_{total} gives a similar $\mu_{eff}(T)$ as the observed. As T is increased, more carriers distribute at higher energy. (c) and (d) are the conductivity production of $\sigma(E)(-\partial f/\partial E)$ with respect to $\sigma(E)$. Increasing T, the production will extend to larger energy region. (e) and (f) are the Fermi level shift against T, for this constant N_{total}.

4.2.3. Gate voltage or carrier density dependences of mobility

It is largely reported that the carrier mobility depends on the gate voltage or the carrier density.[12, 16, 46, 48] In reality, the intrinsic mobility in OFETs should not be affected by extrinsic conditions, such as gate/drain voltage, contact resistance, surface roughness and phonon scattering as well as charge trapping. However, due to the presence of disorders and traps, the apparent mobility (e.g. μ_{eff}) is reduced in comparison with its intrinsic value and shows gate-voltage dependences. So, we address the influences of varying ΔE and α (factor for $D(E)$ distribution relative to DOS, e.g., $0.8\Delta E$ for above calculation where α=0.8). Larger ΔE represents a more disordered system and smaller α means more hopping-like hybridization in the band tails.[45]

In Fig. 4.28a, α=1 indicates a constant diffusivity and thus fully band-like transport in the band, hence the mobility decreases with carrier density due to the degenerate statistics, i.e., $d\mu_{eff}/dN_{total}<0$. As α is much decreased, e.g., α=0.69, hopping-like conduction contributes more to the global transport process. Since the hopping rate depends on the energy barrier that is usually characterized as an activation energy, increasing carriers fill the deep localized states (traps) and, by turn, lower the barrier height.[77] The next induced carriers can hop more efficiently and the mobility increases, i.e., $d\mu_{eff}/dN_{total}>0$. Meanwhile, one should note that the mobility tends to saturate when the traps are filled up, i.e., constant μ_{eff} at high gate voltages. At the intermediate situation, e.g., α=0.85 here, the two transport contributions are comparable and their opposite trend $d\mu_{eff}/dN_{total}$ compensate each other, resulting in a constant mobility over large gate voltage range. Comparing different ΔE (cf. Figs. 4.28a, b), one will find that the disorders increase such an enhancement behavior and the mobility collapses to zero. This is because at low N_{total}, the carriers are mostly lying in the band tails where the transport is nearly accomplished by hopping (keeping α constant), the relative influence of hopping on the overall transport is more important than in ordered system. This effect is shown in Fig. 4.29, where the two limits represent the maximum E_F above which the dielectric (e.g. 50nm SiO_2 with E_{max}=5MVcm^{-1}) will be broken down. These limits are calculated based on the methods presented in our recent work,[71] and the maximum E_F represents the highest carrier density in the layers of organic film next to the gate dielectric at the breakdown gate voltage. As E_F is over zero, the symmetric Gaussian band will give a decreased conductivity (cf. Fig. 4.25) whereas the carrier number remains constant due to degeneracy, and thus the mobility decreases on the right side of the band. In this figure, it is clear that the enhancement only appears for large ΔE.

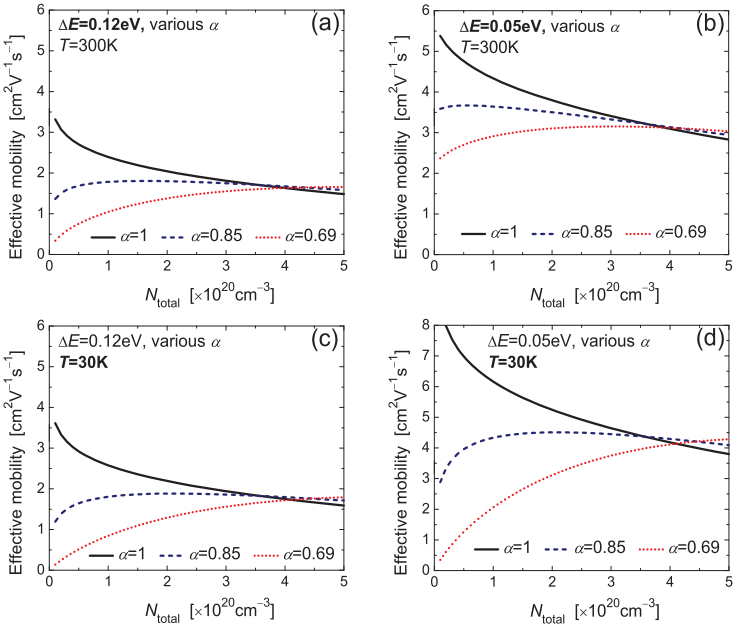


Figure 4.28 | Calculated effective mobility versus carrier density, for three different α. (a) and (b) are for the disordered and ordered system, respectively. (c) and (d) are the same but at 30K.

We also examined the temperature influences. At low T=30K, slight changes occur for large α but for the small α=0.69 (dotted lines), stronger dependences are observed, especially in

the system with ΔE=0.05eV. As discussed above, the μ_{eff} is mainly determined by $\sigma(E_F)$ at low T, increasing N_{total} is actually moving E_F upwards, and thus improving the mobility. The variation of $\sigma(E_F)$ and μ_{eff} with respect to N_{total} is radical in small α case, where the transition of hopping to band-like transport from band tails to band center is very drastic. This impact is even getting greater in small ΔE system since decreasing ΔE sharpens such a transport transition. That's why the mobility becomes strongly carrier density dependent, as seen in Fig. 4.28d. Now we could conclude that the gate-voltage enhanced mobility is due to the hopping-like transport, its impact being stronger in disordered system and at lower temperatures.

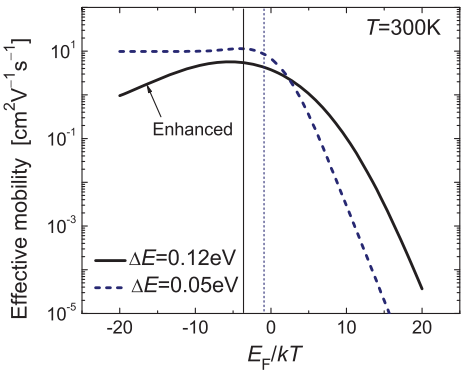


Figure 4.29 | Effective mobility as a function of Fermi energy. The two limits for Fermi level correspond to the dielectric breakdown limit, i.e., the maximum available carrier density in the organic film.

4.2.4. Conclusions

A transport study of the mobility temperature dependence in our TIPS-pentacene OFETs has been conducted. We first examine the issues on the mobility extraction and find that, the field-effect mobility evaluated in saturation regime shows not good enough reliability because a non-linearity of the square root of drain current versus gate voltage is often observed, particularly in short-L transistors and at low T. On the other hand, the low-field mobility extracted by Y function exhibits much better reliability, a good linearity is always obtained, reflecting its greater accuracy for the evaluation of mobility and threshold voltage. This conclusion is confirmed by the effective mobility derived from output conductance with a contact resistance correction, nevertheless Y function is much easier to apply. The temperature dependences of mobility are found to be very similar between the low-field mobility and the effective mobility, whereas the saturation field-effect mobility manifests a different picture at high temperatures. This is indeed related to the mobility extraction method. Furthermore, it is found that the overall transport is significantly limited by the transport in contact region, more pronounced in short-L transistors. The mobility increases with L, and the corresponding activation energy for mobility decreases with L and stabilizes in long-L devices. This inference is further proved by the contact resistance analysis by transfer-line method, a similar variation of mobility and contact conductance against temperature is obtained and a close activation energy is also found for the contact conductance and for the mobility in short-channel transistors. Therefore, the results suggest that an intrinsic transport study in OFETs is better carried out on longer-L transistors with using the more intrinsic mobility, such as the low-field mobility.

The observed carrier mobility remains a constant value at low T and afterwards thermally activated at intermediate T with a small activation energy of 2.3meV, finally the mobility saturates at high T. This variation is well explained by a transport model based on the Kubo-Greenwood integral incorporating a Gaussian-like energy distributed diffusivity in the band. This model also shows the mobility temperature dependences of a band with fully band-like transport and two symmetric localized states tails, corresponding to the practical situation of high quality (single-crystal) and poor quality (amorphous) OFETs, respectively. The former will give a high mobility declining with T and following $\sim T^{-1}$, for not too high carrier density and at not too low temperature due to the approximation of Maxwell-Boltzmann statistics governed by the Einstein relation. The latter will lead to a dominant hopping-like process at low temperatures, and the mobility collapses down to zero with cooling. Increasing T will strongly activate the hopping efficiency, and thus improving the mobility. In the end, we address the carrier density dependences of mobility by varying the disorder and the transport diffusivity level. The gate-

voltage enhanced mobility is indeed attributed to the hopping-like transport, and this influence becomes greater in the disordered system and at lower temperatures.

4.3 THEORETICAL ANALYSIS OF CARRIER MOBILITY IN OFETS *(based on the paper published in Applied Physics Letters 98, 233302, 2011)*[71]

At present, organic electronics attract much attention from industrial and academic research for their unique potential applications such as large area, flexible and low cost. Despite the encouraging progress made in the past two decades, the understanding of carrier transport in organic semiconductors (OSC) and in organic field-effect transistors (OFETs) is still very limited.[44] The carrier mobility is commonly used to explore the carrier transport,[45] with respect to various temperatures, gate/drain voltages and carrier densities.[23, 56] Recently, Li *et al.* presented a model to analyze the field-effect mobility in OFETs.[70] This model is based on the variable range hopping transport with a Gaussian distribution for the density of states (DOS) in the band. However, one need to pay attention to the assumption of zero potential far from the OSC/dielectric interface,[4, 70] here we denote as ψ_0=0. This surface is either exposed in the air without passivation (e.g. bottom-gate configuration) or faced with a relatively much thicker substrate compared to the thin organic film (e.g. top-gate configuration). As a result, the potential at such an open or quasi-free surface is not fixed but rather floating with gate bias, i.e. corresponding to zero surface electric field. This phenomenon could become larger in transistors with thinner OSC film, giving rise to misleading results. Therefore, in this letter the errors arising from this effect is first examined and then an analytical solution is provided. Finally, a mobility theoretical analysis by using the Kubo-Greenwood integral is proposed.

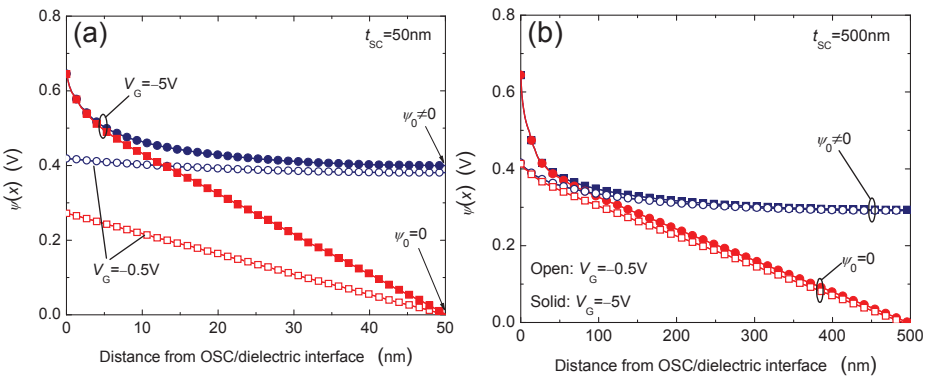


Figure 4.30 | Simulated potential profile from the OSC/dielectric interface to free surface in an OFET with 50nm (a) and 500nm (b) pentacene film, respectively. Here the gate dielectric is 50nm SiO_2 and V_G=–0.5V or V_G=–5V with V_{fb}=0V, T=300K, DOS is Gaussian-like with ΔE=0.1eV.

Fig. 4.30 shows the simulated potential profiles in the organic film of pentacene OFETs with different thickness. One can readily observe a large deviation between the two cases where ψ_0=0, giving a gradual increase of potential from the open surface to the opposite one, whereas, the floating potential (or zero electric field) condition leads to a global potential shift, particularly at small gate voltages (e.g. subthreshold region). The band bending is only significant close to the gate dielectric at high gate voltage (V_G), even less pronounced in thinner film. One may question the impact of such an effect on the surface carrier density and, by turn, on the effective mobility in OFETs.

Next, we address the areal carrier density as a function of gate voltage. As seen in Fig. 4.31a for a film of 50nm, the surface carrier density is quite different in the two cases. Lower areal carrier density is found with the zero potential assumption, or from another point of view, the threshold voltage V_T is shifted to higher absolute value, up to 0.5V, for operating voltage only of −5V. Fig. 4.31c shows the logarithmic plot and a clear difference in the subthreshold region can be recognized. This is due to the fact that increasing V_G accumulates the carriers, but if the

potential at open/quasi-free surface is fixed at zero, the accumulation is only efficient in the immediate vicinity of the gate dielectric. If the potential is left floating at the open surface, the carriers accumulate almost uniformly across the organic film, since the potential moves upwards globally in the film (cf. Fig. 4.30a at V_G=−0.5V). Increasing further V_G, the next induced charges screen the gate field and higher density of carriers accumulate near the dielectric interface. Hence, the carrier transport in subthreshold region is essentially a volume accumulation phenomenon rather than a superficial one, this volume accumulation being more prominent in thinner film. This explains the slight difference observed in a film of 500nm (cf. Figs. 4.31b and 4.31d). In other words, the assumption of ψ_0=0 is nearly valid in the case of very thick film. However, for improving OFETs performance in terms of charge trapping and short-channel effects, thinner organic films will be mandatory.

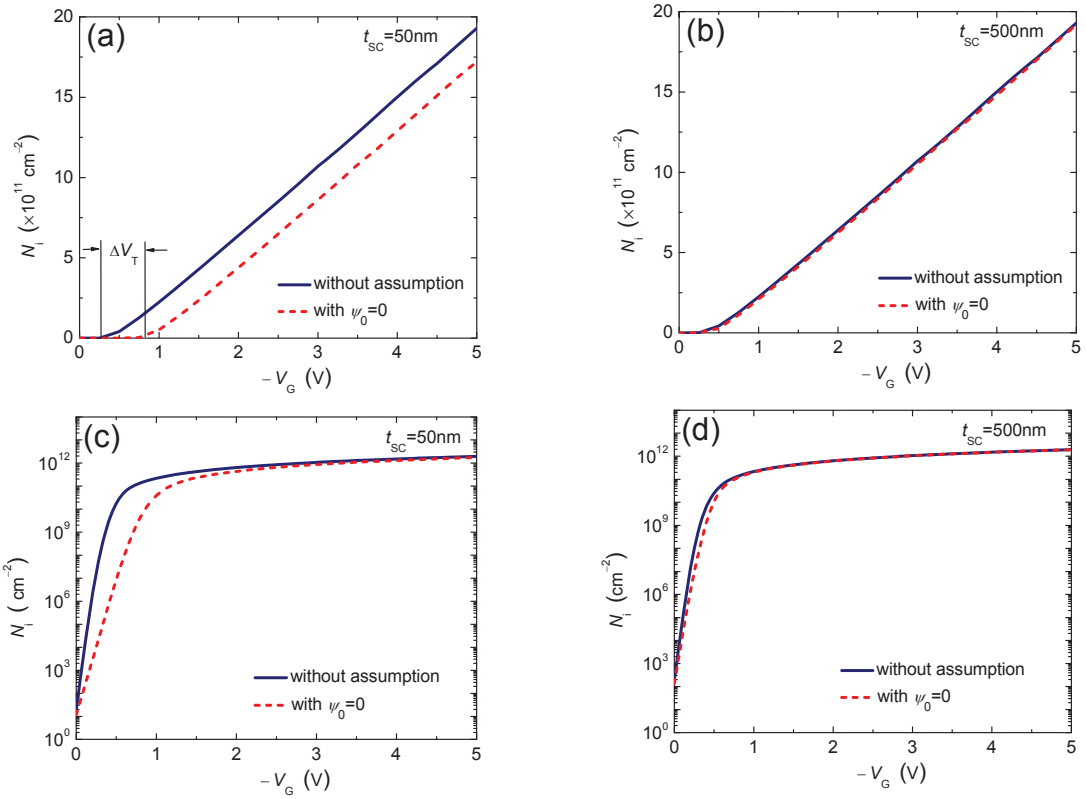


Figure 4.31 | Simulated surface carrier density with respect to gate voltage (a,b), (c,d) are the logarithmic plots to observe the variation in subthreshold region.

Taking into account all these considerations, the local potential in the OSC film $\psi(x)$ can be obtained by solving the Poisson equation:

$$\frac{d^2\psi(x)}{dx^2} = \frac{2q}{\varepsilon_{sc}} \int_{\psi_0}^{\psi(x)} d\psi \int_{-\infty}^{+\infty} N(E) f\left[E - E_{f0} - \psi(x)\right] dE \tag{4.33}$$

where the two surface potentials are denoted as $\psi_s(x=0)$ and $\psi_0(x=t_{sc})$, respectively, with x being the distance from the OSC/dielectric interface, t_{sc} the OSC film thickness, $f(E)=1/[1+\exp(E/kT)]$ the Fermi function, q the electron charge, ε_{sc} the OSC permittivity, E_{f0} the equilibrium Fermi energy and $N(E)$ is the Gaussian distributed DOS with standard deviation ΔE. As a V_G is applied, a potential profile is induced, and, based on Gauss's law, the total areal charge in the organic film can be calculated by integrating once the Poisson equation as $Q_i(\psi_0,\psi_s)=\varepsilon_{sc}d\psi/dx$. From the charge neutrality in the OFET, we have $V_G=V_{fb}+\psi_s+Q_i(\psi_0,\psi_s)/C_i$, where V_{fb} is the flat-band voltage and C_i is the unit area capacitance of gate dielectric. Hence, each V_G corresponds to a potential profile and thus ψ_0 and ψ_s are dependent on V_G. If one

considers the substrate influence (for the quasi-free OSC surface in top-gate configuration), another capacitor like the gate dielectric should be added as:

$$\begin{aligned} Q_i(\psi_0,\psi_s) &= C_i\left(V_G - V_{fb} - \psi_s\right) + C_i'\left(V_G' - V_{fb}' - \psi_0\right) \\ &= \sqrt{2q\varepsilon_{sc}\int_{\psi_0}^{\psi_s} d\psi \int_{-\infty}^{+\infty} N(E) f\left[E - E_{f0} - q\psi(x)\right] dE} \end{aligned} \tag{4.34}$$

where C_i', V_G' and V_{fb}' are related to substrate. As the substrate thickness is usually much larger than that of gate dielectric, i.e., $C_i' \ll C_i$ (with comparable permittivity) and moreover, the back substrate surface is not grounded or polarized, this substrate impact could be neglected. One can readily see from Eq. 4.34 that there are two variables ψ_0, ψ_s depending on V_G. A second integration of the Poisson equation is needed, providing one more equation to solve the system. This can be achieved by integrating the reciprocal electric field across the OSC film such that:

$$t_{sc} = \int_0^{t_{sc}} dx = \int_{\psi_0}^{\psi_s} \frac{dx}{d\psi(x)} d\psi = \int_{\psi_0}^{\psi_s} \frac{\varepsilon_{sc}}{Q_i(\psi_0,\psi)} d\psi \tag{4.35}$$

Combining Eqs. 4.34, 4.35, $\psi_0(V_G)$, $\psi_s(V_G)$ and $Q_i(V_G)$ can be solved numerically for each V_G, as shown in Fig. 4.32 for a 50nm thick pentacene OFET. An equally linear variation of $\psi_0(V_G)$ and $\psi_s(V_G)$ can be seen in the subthreshold region, corresponding to the volume accumulation with a carrier charge Q_i exponentially increasing with V_G. Above threshold, first ψ_0 and then ψ_s saturate, hence Q_i varies linearly with V_G.

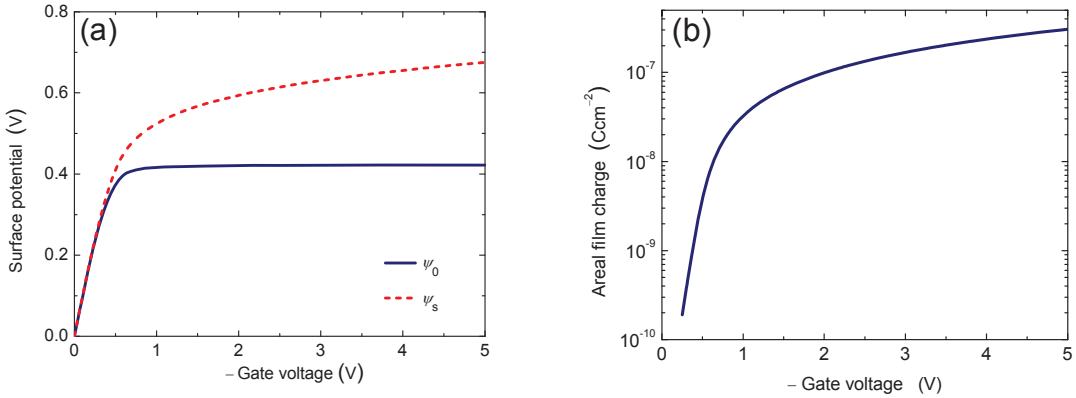


Figure 4.32 | Calculated surface potentials (a) and areal organic film charge (b) versus gate voltage in an OFET with 50nm pentacene film. Here the total band states is 2×10^{21} cm^{-3} with ΔE=0.1eV, T=300K.

In order to calculate the carrier mobility, the total conductivity in the band is first computed by the Kubo-Greenwood integral $\sigma_{total}=\int\sigma(E)(-\partial f/\partial E)dE$,[74] where $\sigma(E)$ is the energy dependent microscopic conductivity and f is the Fermi-Dirac distribution. Because $\sigma(E)=q^2N(E)D(E)$,[68, 75] where $D(E)$ is the diffusivity for each energy, a generic distribution of $D(E)$ is assumed having a Gaussian-like shape with a relatively smaller standard deviation than for the DOS, i.e., $\alpha\Delta E(\alpha\leq1)$. Thus, the diffusivity decreases from band center to band tails as the localized states distributed at the band edges degrade the overall transport from band-like to a more hopping-like process, hence smaller a represents more hopping contribution in the band tails. It should be mentioned that Kubo-Greenwood integral directly offers the total conductivity in the band, irrespective of which kind of transport exactly contributes to the microscopic conductivity. Moreover, note that the generalized Einstein relation applied in Refs.[70, 76] is not necessary here since its effect is already included in the Kubo-Greenwood integral. Therefore, such a mobility calculation offers a much simplified approach and a more general frame for transport analysis. Finally, the sheet conductivity of an OFET channel in linear regime can be obtained by integrating the parallel contribution of each element, for the whole organic film thickness as:

$$G = \int_0^{t_{sc}} \sigma_{total}(x)dx = \int_{\psi_0}^{\psi_s} \sigma_{total}(\psi) \frac{\varepsilon_{sc}}{Q_i(\psi_0,\psi_s)} d\psi \tag{4.36}$$

An effective mobility μ_{eff} can be calculated by G/Q_i. Note that the field-effect mobility μ_{fe} is widely used to investigate the carrier transport, but it might not be appropriate because μ_{fe} is derived from the transistor transconductance which is an extrinsic parameter rather than a pure carrier transport characteristic. For example, a significant increase of transconductance and, thus, of μ_{fe} is observed in subthreshold region but it does not correspond to a real carrier mobility. Furthermore, μ_{fe} can also be affected by contact resistance effect in actual OFETs.[30] On the other hand, the effective mobility applied here is deduced from the channel conductivity and the channel charge, and indeed represents the average carrier mobility.

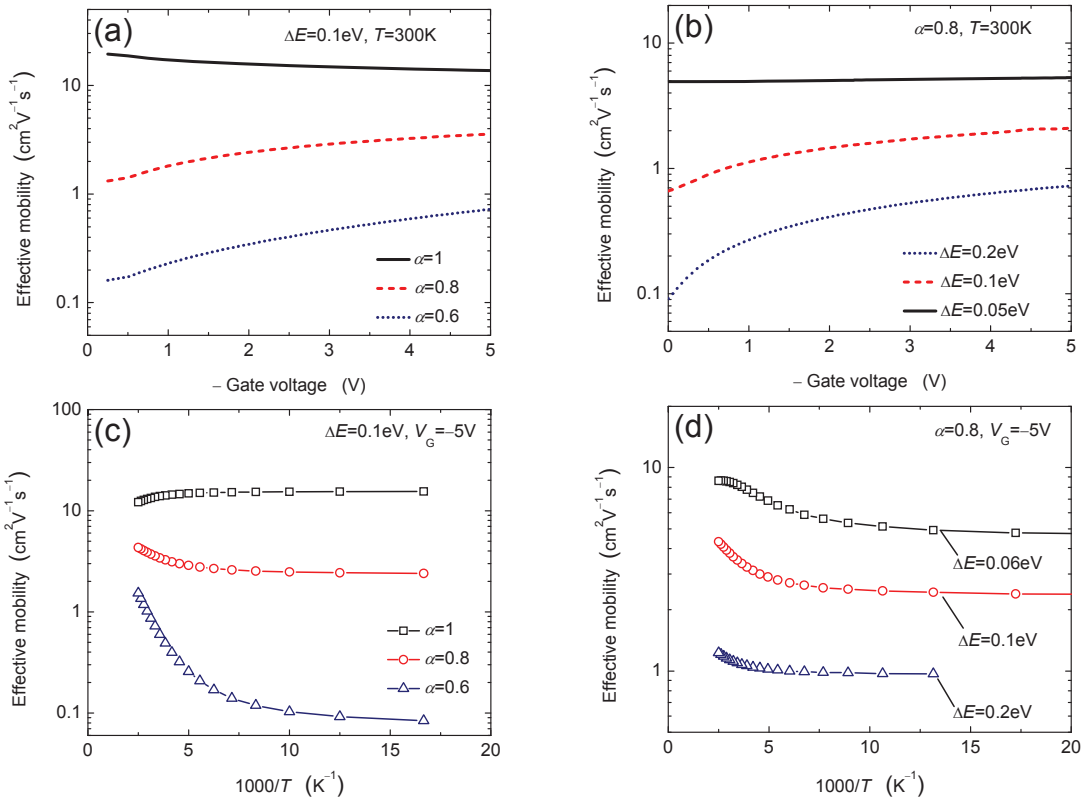


Figure 4.33 | Calculated effective mobility versus gate voltage, at various disorder levels ΔE(a) and transport hybrid levels α(b), for the above OFET. (c,d) are the effective mobility calculated as a function of temperature, at V_G=–5V.

The μ_{eff} in such pentacene OFET is then calculated for various disorder-induced band width and diffusivity degradation levels. In Fig. 4.33a, it is found that μ_{eff} of fully band-like transport (i.e. α=1) decreases with higher gate voltages due to the higher statistics degeneracy, as expected. On the contrary, more diffusivity degradation, i.e. hopping-like contribution (small α=0.6), gives rise to a strongly gate-voltage enhanced mobility,[46] whereas a slowly increasing mobility is observed at intermediate case $\alpha\approx$0.8. Meanwhile, as shown in Fig. 4.33b, more disorder (i.e. larger ΔE with keeping α=0.8) also increases such positive gate-voltage mobility dependence. Note that the mobility enhancement by V_G is clearer at small gate voltages, for which the Fermi level sweeps the band tails with smaller diffusivity i.e. with more hopping transport mechanism. As the gate voltage is increased, the Fermi level moves upward, filling less localized states (e.g. lowering barrier for hopping) and increasing the corresponding diffusivity, thus reducing the influence of hopping. If we hold V_G=−5V and vary the temperature, as seen in Figs. 4.33c and 4.33d, a constant mobility is found at low T.[12, 58, 70] This is because the total band conductivity σ_{total} at low temperature is mainly determined by $\sigma(E)$ at Fermi energy, i.e. $\sigma(E_F)$, resulting in a single-energy contribution nearly independent of temperature. Increasing T breaks this situation with broadening the energy distribution of carriers and $\sigma(E)(-\partial f/\partial E)$ term in the Kubo-Greenwood integral, activating the mobility. This activation is stronger for more degraded

diffusivity (i.e., larger hopping barrier), but not so obvious for various band width (disorder) levels, as seen in Fig. 4.33d. Increased disorder only reduces the mobility because the Fermi level is decreased. One may notice the mobility saturation or even decrease at high T for small ΔE=0.06eV. This is due to the fact that at high T, the Fermi level moves towards midgap and Boltzmann's statistics prevails, implying more band-like transport with a decreasing mobility with T.

In summary, a theoretical analysis of carrier mobility in OFETs has been presented. In order to obtain the effective mobility, the channel charge is first calculated with taking into account the carrier distribution throughout the organic film, where the deviation originated from the zero open/quasi-free surface potential assumption is studied. This assumption causes a lower areal carrier density, particularly in thinner-film transistors and in subthreshold region. Next, the channel conductivity is integrated in the organic film by using the Kubo-Greenwood integral, which gives the band conductivity from a microscopic transport viewpoint and thus provides a general framework for mobility calculation in different disorder and diffusivity levels, with respect to gate voltage and temperature.

4.4 CONCLUSIONS

In this chapter, a modeling work on OFETs' DC characteristics has been first presented. This is based on a 1-D analytical solution of Poisson's equation for the organic film in organic transistors, by which the potential profile and the carrier concentration in the organic film can be derived. Combing the Gauss law, one can calculate the charge per unit area in the organic film at each gate voltage, and thus obtaining the drain current in linear regime for an organic transistor. This model reveals the importance of the open surface on the overall carrier transport, the subthreshold transport in the film is a volume phenomenon rather than the widely believed superficial one also because of the intrinsic organic semiconductors; the band bending is only significant near the gate dielectric as a high gate voltage is applied. The calculated results well account for the measurement data of pentacene OFETs however the bulk traps cause a large deviation in fitting to the experimental data of TIPS-pentacene OFETs. We thus performed simulations on traps, with different location (surface/bulk), different energy distribution of DOS and donor/acceptor-like, the analytical solution involving shallow bulk traps introduced from the open surface well explains the experimental data.

Next, we focused on the carrier transport in organic semiconductors and organic transistors. Three mobilities are extracted against temperature by different method in our TIPS-pentacene OFETs, the low-field mobility exhibits the best reliability and easy of use, particularly at low temperatures and for short-channel transistors. The analysis of OFETs having diverse channel lengths indicated that the overall carrier transport in short-channel OFETs (e.g. L=5μm) is nearly dominated by the transport in the contact vicinity, suggesting that a more intrinsic transport study in organic semiconductor is better carried out on the relatively longer-channel devices. The observed temperature dependences of mobility are well explained by a mobility model using Kubo-Greenwood integral. A constant diffusivity in the band would result in a high mobility decreasing with temperature, implying inherent band-like transport in delocalized states. A window-like diffusivity with two symmetric mobility edges would lead to a fully localized carrier transport at low carrier density and at low temperatures, the mobility decreases to zero. Increasing temperature activates the carrier distribution in the band and improves the hopping efficiency, manifesting a thermally activated mobility with large activation energies. A generic Gaussian-like diffusivity in the band gives a smooth transition of hopping transport to band-like transport from band tails to band center. It well explains the observed mobility variation with temperature in the long- and short- channel OFETs, in the latter the disorder level and defect density are higher. One also addressed the gate-voltage or carrier density dependent mo-

bility, and found that it is due to the hopping transport. This impact is more pronounced in the disordered system and at lower temperatures.

In the end, we analyzed the carrier mobility in organic transistors with considering the charge distribution in the film as discussed in the first section. The simulation results indicated that the assumption of zero potential at free/open surface will give rise to a large deviation in the threshold voltage and subthreshold slope from the real situations, where the floating surface potential at free surface corresponds to a volume transport in subthreshold region. This impact is even getting greater in the OFETs with thinner organic film. Taking account of this effect, the whole conductivity in the organic film is calculated by using the Kubo-Greenwood, and thus obtaining the effective mobility for all carriers. This analysis enables a mobility study at each gate voltage, instead of the previous one by using the carrier density for a bulk of organic semiconductor. So the effective mobility is analyzed with respect to the gate voltage and temperature, for different delocalized-localized states hybridization level and different disorder level.

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Chapter 5
Low-frequency noise

The low-frequency noise (LFN) measurements are known as a useful tool to investigate the carrier transport in the channel and the dielectric quality in terms of trap density. This technique has been widely applied to organic transistors, offering an insight into the trap density which nowadays is an important issue in OFETs due to the commonly existing defects and impurities.

5.1 ELECTRONIC NOISE IN MICROELECTRONIC DEVICES

Before moving to the LFN measurements in devices, we briefly introduce the basic theory about the electronic noises and their analysis methods.

■ Power spectral density (PSD)

A nominal static electronic signal (voltage or current) microscopically is not stable but rather fluctuates around a fixed value. This fixed value is the mean value and the small fluctuation at a time point is the variance. These microscopic fluctuations cause the electronic noise. To analyze noise, the Fourier transform is commonly used, and it could change the analysis from time domain to frequency domain.

If a signal is continuous and has a finite energy (i.e., it could be square integrable), its spectral density $\Phi(\omega)$ is the square of the continuous Fourier transform as:

$$\Phi(\omega) = \left| \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{+\infty} f(t) \cdot e^{-j\omega t} dt \right|^2 = \frac{F(\omega) \cdot F^*(\omega)}{2\pi} \tag{5.1}$$

If this signal could be seen as a stationary random process, namely the sampled signal doesn't depend on the sampled time; its power spectral density (PSD) $S(f)$ is just the Fourier transform of its autocorrelation function $R(\tau)$ as:

$$S(f) = \int_{-\infty}^{+\infty} R(\tau) \cdot e^{-2\pi i f \tau} d\tau \tag{5.2}$$

PSD represents the signal power or energy per Hz, hence it indicates the signal power distribution with respect to frequency. The signal power equals to the dissipated energy on a 1 ohm resistive load, hence its unit is W/Hz. In real application, because the power is often denoted by the square of the real signal value either in voltage or in current, hence the unit of PSD often is V^2/Hz or A^2/Hz, corresponding to the two forms of PSD: S_I and S_V.

■■ PSD in S_I

If the PSD is measured from a signal of current (e.g., I_D), the accordingly PSD is S_{ID} with the unit of A^2/Hz.

■■ PSD in S_V

If the PSD is measured from a signal of voltage (e.g., V_G), the accordingly PSD is S_{VG} with the unit of V^2/Hz.

Recall the ohms law: $V=I\times R$ or $V=I/g$, we have:

$$S_{V_D} = S_{I_D} / g_d{}^2 \text{ or } S_{V_G} = S_{I_D} / g_m{}^2 \tag{5.3}$$

Finally, it should be noted that PSD is a function in frequency domain not in time domain.

■ Thermal noise

Thermal noise is caused by the brown movement of the charge carriers in a resistive medium. It is independent of the applied voltage and also independent of frequency, thus thermal noise is a white noise, i.e., its PSD is constant over a large range of frequency (typically from few Hz to MHz). If the load is a resistance with value of R and the noise is measured from the voltage between two electrodes, the thermal noise PSD reads:

$$S_{V_R} = 4kT \times R \tag{5.4}$$

For a transistor operating in linear regime, the thermal noise PSD of the drain current is:

$$S_{I_D} = 4kT \times G_D \tag{5.5}$$

where G_D is the output conductance. If this transistor works in saturation regime, the thermal noise PSD of I_D has an expression very similar to that for the shot noise as:[1, 2]

$$S_{I_D} = 2qC \times I_{Dsat} \tag{5.6}$$

where C is a constant. So it is often confused to be regarded as a shot noise. Note that in transistors the thermal noise attains maxima at V_D=0V.

■ Shot noise

This type of noise originates from the fact that the current flowing across a junction is not smooth, but is incorporated of individual charge carriers arriving at random times. Such a non-uniform or quasi-discrete flow leads to broadband white noise, and it becomes worse with increasing the flowing current. Thus the associated PSD is:

$$S_I = 2q \times I \tag{5.7}$$

■ Generation-recombination noise

The mechanism of generation-combination (G-R), i.e. the charge capture/release by the traps which locate in the semiconductor bulk, causes fluctuations of the carrier number in the band and thus fluctuation in the resistance.

■ Flicker noise (1/*f* noise)

There have been more than 80 years since the first observation of 1/*f* noise in vacuum tube; 1/*f* noise is often called as flicker noise since it was observed from the plate current. The term of 1/*f* is resulted from the fact that its spectrum varies inversely with frequency as $1/f^{\alpha}$, where the exponent α is very close to unity (α=1±0.2).

1/*f* noise is found in numbers of situations, such as in all materials and in all electronic devices, mechanical, biological, geological and even musical systems. 1/*f* noise generally dominates the overall noise spectrum at low frequencies. Up to now, there has not been a universal explanation for the origination of 1/*f* noise but there have been two theories, which well account for the formation of 1/*f* noise in microelectronic devices, i.e. the carrier number fluctuation model (Δn) proposed by McWhorter and the mobility fluctuation model($\Delta\mu$) proposed by Hooge.

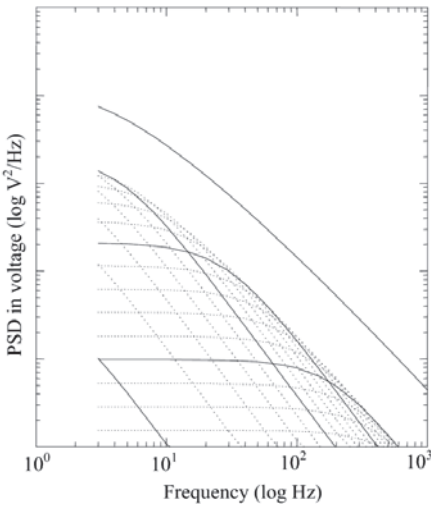


Figure 5.1 | Formation of the spectrum of 1/f by superposition of several Lorentz spectrums.

■■ Carrier number fluctuation model

In this regime, the drain current fluctuation is due to the fluctuation of the mobile charge number in the channel near the interface of semiconductor/dielectric resulted from the dynamic

charge capture/release by the slow traps distributed in the dielectric. Note that this charge trapping/detrapping is different from that for G-R noise because the traps responsible for G-R noise lie in the semiconductor bulk not in the gate dielectric.

In consequence, taking into account the mobility variation $\delta\mu_{eff}$ induced by the mobility dependence of the insulator charges, thus the drain current fluctuation reads:

$$\begin{aligned}\delta I_D &= \delta V_{fb}\frac{\partial I_D}{\partial V_{fb}}\bigg|_{\mu_{eff}=const} + \delta\mu_{eff}\frac{\partial I_D}{\partial \mu_{eff}}\bigg|_{V_{fb}=const} \\ &= -g_m\delta V_{fb} - \alpha I_D\mu_{eff}\delta Q_{it}\end{aligned} \tag{5.8}$$

where α is the coulomb diffusion coefficient ($\approx 10^4 Vs/C$), δV_{fb} and δQ_{it} are the fluctuation of the flat-band voltage and the interface charge, respectively, with $\delta V_{fb}=-\delta Q_{it}/(WLC_i)$. Therefore, the normalized PSD written as:

$$\frac{S_{I_D}}{I_D^{\,2}} = \left(1+\alpha\mu_{eff}C_i\frac{I_D}{g_m}\right)^2\frac{g_m^{\,2}}{I_D^{\,2}}S_{V_{fb}} \tag{5.9}$$

$$S_{V_G} = \left(1+\alpha\mu_{eff}C_i'\frac{I_D}{g_m}\right)^2 S_{V_{fb}} \tag{5.10}$$

Here $S_{V_{fb}} = S_{Q_{it}}/(WLC_i^{\,2})$ and $S_{Q_{it}}(C/cm^2Hz)$ is the spectral density of the fluctuation of the interface areal charge. From Eq. 5.10, it is clear that if $\alpha\approx 0$, i.e., mobility is not sensitive to the trapped charges, $S_{V_G}\approx S_{V_{fb}}$ and thus there is only the last term in Eq. 5.9 left. Note that Eqs. 5.9 and 5.10 are always valid at small I_D and high I_D (i.e. linear and saturation regime).

If a transistor works in linear regime and in strong inversion, one can replace I_D by $(W/L)\mu_{eff}Q_iV_D$ and g_m by Eq. 3.24. Eq. 5.10 becomes:

$$S_{V_G} = \left(1+\alpha\mu_{eff}C_i'\frac{I_D}{g_m}\right)^2 S_{V_{fb}} = \left[1+\alpha\mu_0C_i'(V_G-V_T)\right]^2 S_{V_{fb}} \tag{5.11}$$

The noise PSD of V_G exhibits a parabolic relationship with the gate voltage. Next, we present the analysis of $S_{V_{fb}}$ basing on the different trapping mechanism and its resultant $1/f$ noise.

■■■ ***Trapping by tunnel process:*** In general, the $S_{Q_{it}}$ depends on the physical mechanism of charge trapping by the slow traps in gate insulator. In the case of a tunneling process, the trapping probability decreases exponentially with the depth of traps in the dielectric x, so the $S_{V_{fb}}$ is:

$$S_{V_{fb}} = \frac{q^2kT\lambda N_t}{WLC_i^{\,2}f^{\gamma}} \tag{5.12}$$

where f is the frequency under study, γ is the characteristic exponent which is close to unity, λ is the tunnel attenuation distance ($\approx 0.1nm$) and N_t is the volumetric trap density in the gate dielectric($eV^{-1}cm^{-3}$).

■■■ ***Trapping by thermally activated process:*** In this case of trapping process, the trapping probability decreases exponentially with the cross section activation energy E_a, the $S_{V_{fb}}$ reads:

$$S_{V_{fb}} = \frac{q^2k^2T^2N_{it}}{WLC_i^{\,2}f^{\gamma}\Delta E_a} \tag{5.13}$$

where ΔE_a is amplitude of the activation energy dispersion, N_{it} is the surface trap density in the gate dielectric($eV^{-1}cm^{-2}$).

The two trapping processes giving $1/f$ nature in spectrum is due to the uniform distribution of the time constant in log scale (cf. Fig. 5.1). A number of Lorentz spectrums are superimposed together, leading to a $1/f$ overall spectrum at low frequencies. Note that the $S_{V_{fb}}$ in the case of

thermally activated process more strongly depends on the temperature ($\sim T^2$) than in the case of tunneling process ($\sim T$).

■■ Hooge mobility fluctuation model

In contrast to the theory of McWhorter, Hooge proposed that the $1/f$ noise of the drain current is due to a volume phenomenon of the carrier mobility fluctuations resulted from the phonon scattering. As a result, the flicker noise amplitude is inversely proportional to the total carrier number in the device. The normalized PSD of I_D is:

$$\frac{S_{I_D}}{I_D^{\ 2}} = \frac{q\alpha_H}{WLQ_i f} \tag{5.14}$$

where α_H is the Hooge parameter, a empirical parameter is around 10^{-5} for classical silicon MOSFETs. So the S_{V_G} is :

$$S_{V_G} = \frac{S_{I_D}}{I_D^{\ 2}} \frac{I_D^{\ 2}}{g_m^{\ 2}} = \frac{q\alpha_H}{WLQ_i f} \times \frac{I_D^{\ 2}}{g_m^{\ 2}} \tag{5.15}$$

If the transistor operates in linear regime and in strong accumulation, thus $Q_i \approx C_i(V_G - V_T)$ and $I_D / g_m = (V_G - V_T)[1 + \theta(V_G - V_T)]$, we have :

$$S_{V_G} = \frac{q\alpha_H}{WLC_i f}(V_G - V_T)[1 + \theta(V_G - V_T)]^2 \tag{5.16}$$

we will see that the S_{V_G} is proportional to $(V_G - V_T)$.

■■ Diagnosis of the low-frequency noise sources

Once the observed LF noise shows $1/f$ type spectrum, the conventional LFN sources diagnostic process can be conducted. Because there are two possible theories to explain the LF noise sources in transistors, so it is necessary to distinguish which one is dominant, McWhorter or Hooge.

First, the normalized S_{Id}/I_D^2 for a fixed frequency is plotted with respect to I_D in log-log scale.[2] And then, the variation of $S_{Id}/I_D^2(I_D)$ is compared with that of $(g_m/I_D)^2(I_D)$ also in log-log scale by adjusting a constant factor. If the two curves could be well superimposed, one can conclude that the carrier number fluctuations model dominates and that adjusting factor corresponds to the trap density (cf. Eq. 5.12). At the same time, if the input gate voltage noise PSD S_{V_G} exhibits a parabolic dependence on V_G in strong inversion (strong accumulation for OFETs here), one can say that the correlated mobility fluctuations cannot be disregarded, i.e. α>>1. On the other hand, if the $S_{Id}/I_D^2(I_D)$ varies inversely with the drain current from weak inversion to strong inversion, it indicates that the Hooge mobility fluctuations are responsible for the observed $1/f$ noise. This phenomenon is often observed at small drain current since the carrier density is low and the relative LFN level is higher.

In general, the carrier number fluctuations model is found to be valid in the devices operating in surface mode. On the contrary in the devices working in volume mode, e.g. nano wire, the Hooge mobility fluctuations model usually prevails.

■ Noise measurement system

A system 3PNMS (Programmable Point Probe Noise Measuring System) controlled by the software of NOISYS is used for the LF noise measurements in this thesis. This

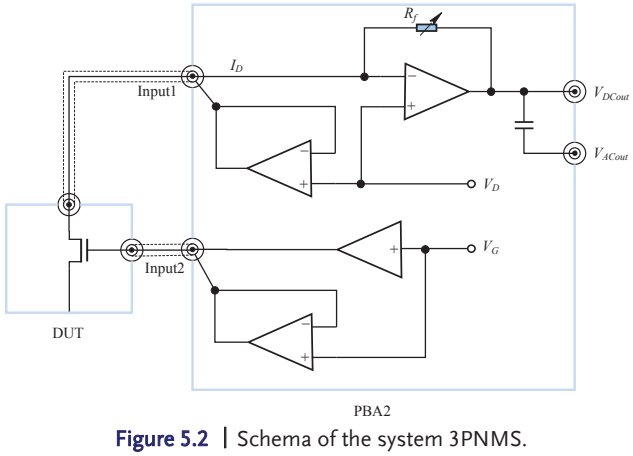


Figure 5.2 | Schema of the system 3PNMS.

system allows us to obtain the static (DC) and dynamic (AC) data (i.e., noise) simultaneously. As shown in Fig. 5.2, a programmable amplifier with variable gain by adjusting the feedback resistance R_f, the Input 1 current of DUT (Device Under Test) is measured, here it is the drain current of a tested transistor. After a fast Fourier transform, the PSD of the measured signal (S_{Id} here) is obtained.[3]

5.2 ORIGIN OF LFN IN PENTACENE OFETS (*based on the paper published in Solid-State Electronics, 61, 106, 2011*)[4]

5.2.1. Introduction

Organic materials (OMs) find ever-growing use as active elements in a new generation of (opto) electronic devices. Despite of low carrier mobility in OMs, they have already demonstrated an extraordinary potential for cheap, low-end and all plastic electronics for such applications as large-area light-emitting displays, disposable circuits for product labeling, or light-weight photovoltaic cells,[5] in short, applications where high speed of electronics elements is not essential. The progress in development of organic field-effect transistors (OFETs)[5, 6] is seriously impeded by a poor understanding of electrical transport mechanisms in organic materials. Another important but unresolved problem in the OFET studies is that of electrical contacts,[7, 8] involving charge injection from a metal into a low-conducting medium, often complicated by the presence of traps and disorder. Low frequency noise (LFN) analysis is known as an elegant tool to investigate dielectric quality and thus to understand the channel transport mechanisms. So far, few works on OFETs' LFN have been reported.[9-14] Different results were observed and explained due to the various organic materials used as semiconductor, such as polycrystalline-like small molecular semiconductors [9, 12, 13] or amorphous-like polymer semiconductors. [11, 12, 14] The Hooge mobility fluctuations were asserted in some of the above mentioned works, in which somewhat narrow current spanning was utilized. However it might be misunderstood since a similar dependency could also occur in the carrier number fluctuations model, thereby a conclusion drawn over several current decades is required. On the other hand, the contact resistance nowadays is a crucial issue in OFETs;[7, 8] its contribution to LF noise has already been discussed in refs, [9, 10, 12] but an explicit investigation has not been addressed.

This paper belongs to that category; namely we address here the problem of LF noise generation in the pentacene OFETs. The incentive for this research was given by our early tests on LFN measurements carried out on OFETs that demonstrated unusually high noise level in OFETs with the gate surface area of the order a millimeter square. The LFN will therefore be one of the important problems to eliminate, once the miniaturization of the devices sets on.

In this paper we first discuss briefly the device fabrication and then we present the conventional LFN diagnosis procedure involving two classical models of LFN generation via Hooge mobility fluctuations and carrier number fluctuations. Next, we shall discuss LFN experimental results obtained on pentacene OFETs which have different configurations, stressing the importance of the contribution from the contact resistance. It should be emphasized that the properly normalized LFN data scale with the gate surface area in the region of predominance of the carrier number fluctuation mechanism (at sufficiently low I_D) and does not in region of higher I_D values. That was a departing point for interpreting the data via the number fluctuation model supplemented by the contact resistance noise.

5.2.2. Device fabrication

The devices used in this work were fabricated on heavily doped Si (100) wafers covered with a 50nm thick SiO_2 layer. Ultimately they serve as the gate electrode and the gate insulator, respectively. After cleaning the surface with organic solvents and acids, a self-assembled

monolayer of octadecyltrichlorosilane was formed on the SiO_2 surface in order to reduce the concentration of interface states. Bottom contact (BC) and top contact (TS) OFETs were fabricated. In the former, the source and drain electrodes were formed directly on the SiO_2 surface, by a sequential evaporation of 5-nm-thick MoO_3 and 35-nm-thick gold through a metal mask, following which a pentacene (Aldrich, purified using temperature gradient sublimation) layer was vacuum-deposited (rate of 0.01 nm/s at room temperature, final thickness of 50nm). In the TC devices the pentacene layer was deposited first and then the source and drain electrodes were made by thermal evaporation of Cu through a mask.

5.2.3. Modeling of flicker noise

The $1/f$ noise or flicker noise in the FETs is known to comprise two major components, originating from:

(I) Δn carrier number fluctuations (McWhorter),[15] where the trapping/release of carriers near the dielectric/semiconductor interface modulates the flat-band potential via:[16]

$$\delta_{Vfb} = -\delta_{Qit}/(WLC_i) \tag{5.17}$$

where δV_{fb} and δQ_{it} are the fluctuations of the flat band voltage and the surface trapped charge, respectively. W and L are the channel width and length, respectively. C_i is the unit area capacitance of gate dielectric (F/cm^2).

This fluctuation from the flat-band voltage gives rise to a fluctuation of the drain current, δI_d by the relation:

$$\delta_{Id} = -g_m \times \delta_{Vfb} \tag{5.18}$$

where g_m is the transconductance. Taking into account the correlated mobility fluctuation $\delta\mu_{eff}$ due to the modulation of the scattering rate induced by the interface charge fluctuations, a more complete expression for the drain current fluctuations reads:[17]

$$\delta_{Id} = -g_m \times \delta_{Vfb} - \alpha I_D \mu_{eff} \delta_{Qit} \tag{5.19}$$

where α is the Coulomb scattering coefficient. Hence the normalized power spectral density (PSD) of drain current fluctuations, $S_{Id}/I_D{}^2$ can be written as: [17]

$$\frac{S_{Id}}{I_D{}^2} = \left(1 + \alpha\mu_{eff} C_i \frac{I_D}{g_m}\right)^2 \left(\frac{g_m}{I_D}\right)^2 \times S_{Vfb} \tag{5.20}$$

where S_{Vfb} is the PSD of the flat-band voltage fluctuations. The input gate voltage noise defined as $S_{VG} = S_{Id}/g_m{}^2$ becomes for strong inversion or strong accumulation as:

$$S_{V_G} = S_{V_{fb}} \left[1 + \alpha\mu_0 C_i (V_G - V_T)\right]^2 \tag{5.21}$$

where μ_0 is the low-field mobility and V_T is the threshold voltage. Here $S_{Vfb} = S_{Qit}/(WLC_i{}^2)$, where S_{Qit} is the PSD of interface charge fluctuations per unit area (C^2/Hz/cm^2).

Upon the assumption that flat band fluctuations are induced by charge capture/release on traps uniformly distributed in the dielectric's volume, via direct tunneling, whose rate decreases exponentially with the distance from the semiconductor/dielectric interface, integration of individual fluctuations gives the following result for S_{Vfb} [15, 17]

$$S_{V_{fb}} = \frac{q^2 kTN_{ST}}{WLC_i{}^2 f} \tag{5.22}$$

where q is the electron charge, kT is the thermal energy; N_{ST} is the surface trap density, and f is the frequency under study. Note that in Eqs. 5.19, 5.20 and 5.21, in the absence of correlated mobility fluctuations (α=0), $S_{VG} = S_{Vfb}$, which yields the relation: [17]

$$\frac{S_{I_d}}{I_D{}^2} = \frac{q^2 kTN_{ST}}{WLC_i{}^2 f} \times \left(\frac{g_m}{I_D}\right)^2 \tag{5.23}$$

It is worth emphasizing that, in our case, given the back gate configuration of the pentacene transistors with open top surface, the surface trap density N_{ST} appearing in Eqs. 5.22 and 5.23 should be regarded as an effective surface density, comprising all the trap states

distributed at both bottom and top pentacene interface and/or in the bulk.

(II) $\Delta\mu$ mobility fluctuations (Hooge).[18] In this model, the carrier mobility fluctuations originate from the carrier-phonon scattering and the normalized S_{Id} is expressed through a phenomenological expression,[17]

$$\frac{S_{I_d}}{I_D^{\,2}} = \frac{\alpha_H}{WLn_s f} \propto 1/I_D \tag{5.24}$$

where n_s is the surface carrier density and α_H is the Hooge parameter ($10^{-6}<\alpha_H<10^{-3}$ for classical silicon MOSFETs and semiconductor).

The analysis of the LFN data is often based on the use of Eqs. 5.20-5.21 and 5.23-5.24. The normalized drain current PSD, S_{Id}/I_D^2, taken at a sufficiently low f, assuring the dominance of the flicker noise, is plotted as a function of I_D in the log-log scale.[17] If S_{Id}/I_D^2 varies with the dependence of $(g_m/I_D)^2$ (cf. Eq.5.23), one can conclude that the carrier number fluctuations dominates. If the associated input gate voltage noise S_{VG} shows a parabolic dependence with gate voltage at strong inversion, correlated mobility fluctuations should be involved (see Eq. 5.21). On the other hand, if S_{Id}/I_D^2 varies as I_D^{-1} from small to high biasing conditions, one can assert that the Hooge mobility fluctuations model accounts for the LFN data.

As mentioned in the introduction, most of the publications on LFN in OFETs use the Hooge $\Delta\mu$-fluctuations model in data interpretation.[9, 11, 12, 19] A closer inspection shows that the presented data were taken mainly over a range of current intensities of less than 2 decades, which is hardly adequate for drawing significant conclusions as to the general noise dependence on the current. In a limited range of I_D intensities, a region where S_{Id} follows the dependence of I_D^{-1} can always be found, which often serves as a justification for the application of the Hooge $\Delta\mu$-fluctuation model. Furthermore, the Hooge parameter was used for evaluating the noise level in the literature,[9, 11, 12, 19] and it was found to be as high as 10~100.[9, 12] However up to now, no attempt has been made to explain the origin of such high values of α_H, nor the mechanism of the Hooge $\Delta\mu$-fluctuations in organic materials.

Compared to Hooge mobility fluctuations model, the carrier number fluctuations model was rarely reported to be valid in OFETs.[10, 20] This might be due to the amorphous or poly-crystalline organic semiconductor, where the carriers transport is different from that in conventional silicon MOSFETs. In our pentacene devices, we will see that the LF noise is well in agreement with the carrier number fluctuations model. A special feature of this model is to provide the trap density, which is an important issue in the OFETs domain. Moreover, this model concerns the real physical phenomena and thus allows us to understand the carrier transport mechanisms in the channel.

5.2.4. Experimental results and discussions

■ Δn model versus Δμ model

A typical PSD of drain current fluctuations S_{Id} for a TC OFET is plotted in Fig. 5.3 at various gate voltages *versus* frequency f. Similar data were obtained in the BC devices (not shown). The system noise has been subtracted from measured noise for each gate voltage. One can readily see, at sufficiently high drain current I_D, the LF noise shows a clear $1/f$-type spectral dependence. The upswing of PSD at high frequencies is due to the instrumental limitation. It only can be seen on the noise floor and does not affect the effective noise in the devices at higher

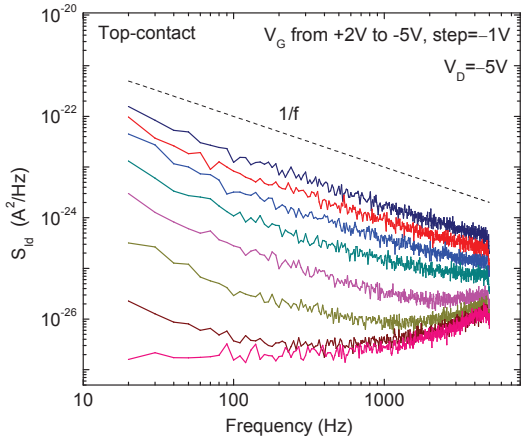


Figure 5.3 | Typical PSD of drain current fluctuations observed in a TC OFET at various gate voltages, the dashed line indicates the slope of $1/f$.

biasing conditions.

In order to determine current regions where model I or II dominate, the normalized PSD of the drain current fluctuations S_{Id}/I_D^2 at f=20Hz is plotted with respect to I_D in log-log scale, as shown in Fig. 5.4 (circles). As seen in the figure S_{Id}/I_D^2 varies as $(g_m/I_D)^2$ over 3-4 decades of I_D intensities, both in TC and BC OFETs. This clearly means that the LF noise originates from carrier number fluctuations (Eq. 5.23) in the whole region of I_D intensities in question. We will see below that the correlated mobility fluctuations could be neglected. On the other hand, the Hooge mobility fluctuation model predicts that S_{Id}/I_D^2 should varies as $1/I_D$ (broken line), and it clearly cannot account for the LF noise variation.

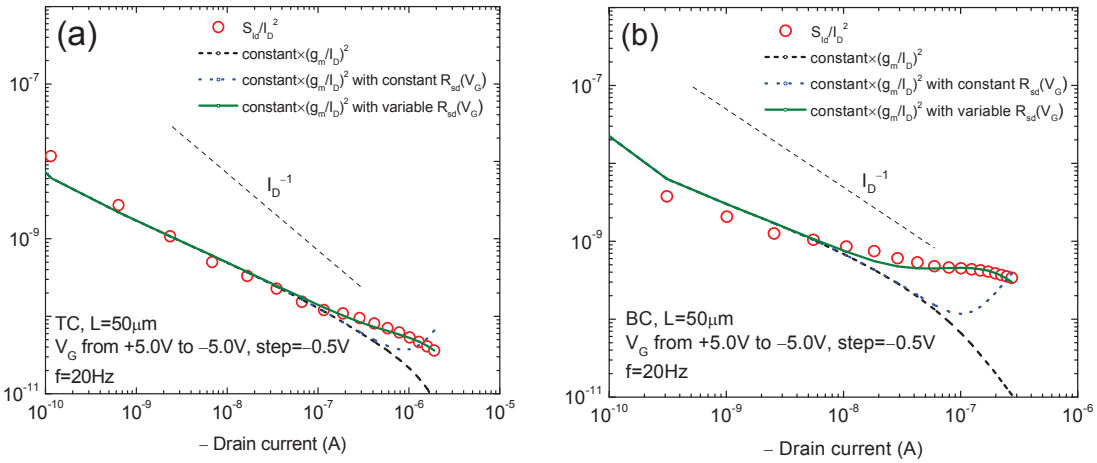


Figure 5.4 | Drain current intensity, I_D, variation of the normalized PSD S_{Id}/I_D^2 at f=20Hz and of *constant*×$(g_m/I_D)^2$, where g_m is the transconductance, measured in TC (a) and BC (b) devices. The value of the *constant* is adjusted to fit the data.

The surface trap density values N_{ST} extracted using Eq. 5.23 from the data are listed in Table 5.1 for several samples. As seen, the N_{ST} values for the BC OFETs are 10 times higher than that in their TC counterparts.[7, 20, 21] This is consistent with a poorer crystal structure in the contact region in BC OFETs, which could lead to higher N_{ST} values. Note that the surface trap densities obtained in these pentacene OFETs are much higher than that in their silicon counterparts, where the surface trap density seldom exceeds 10^{10}/eVcm^2.

In order to investigate the nature of the states responsible for the measured LFN, we evaluated separately the surface states density near/at the interface N_{SS} from the sub-threshold slope of the $I_D(V_G)$ characteristic.[22, 23] The obtained N_{SS} values are also listed in Table 5.1 and are seen to be close to the N_{ST} values determined from the LFN analysis, which implies that the same states are likely involved. But the N_{ST} values in BC devices are much higher than their N_{SS} values, whose magnitudes remain of the same order as the TC devices. It confirms that the additional trap states in the vicinity of contacts induced by the process defects increase the overall equivalent surface trap density.

■ Contact noise contribution

As seen in Fig. 5.4, S_{Id}/I_D^2 deviates upwards from the $(g_m/I_D)^2$ dependence at higher I_D intensities. Such an upswing in the $S_{Id}/I_D^2(I_D)$ data has been often observed in silicon MOSFETs[24] and has also been reported in OFETs.[9, 10, 12] In those devices it was interpreted by the presence of Δn-$\Delta\mu$ correlated noise (expressed by the second term in the first parenthesis of Eq. 5.20) and by the noise generated in series (access) resistance R_{sd}. The latter can give in some cases a change in slope of the $S_{Id}/I_D^2(I_D)$ function from negative to positive. It should be noted that the correlation effects in the OFETs should be very small because the correlation term in Eq. 5.20 contains the carrier mobility. The mobility in OMs is many orders of magnitude smaller than in classical semiconductors, however, the contact resistance in OFETs is much higher than

in conventional MOSFETs. We attribute therefore the upward shift in the $S_{Id}/I_D^2(I_D)$ function observed in OFETs to the noise generation in access (contact) resistance, $R_{sd,}$ alone.

Generally the data are simulated by an expression where the normalized PSD of Eq. 5.23 (channel) is complemented by an additional R_{sd}-dependent term,[24]

$$\frac{S_{I_D}}{I_D^2} = \left(\frac{S_{I_D}}{I_D^2}\right)_{channel} + \frac{S_{R_{sd}}}{R_{sd}^2} \times R_{sd}^2 \times \left(\frac{I_D}{V_D}\right)^2 \tag{5.25}$$

where S_{Rsd}/R_{sd}^2 is the normalized PSD of the contact resistance, which characterizes the intrinsic contact LF noise.

The availability of TC and BC devices, significantly differing in the R_{sd} values, allows us to link their magnitude to that of the second term in Eq. 5.25. In fact, as it follows from Fig. 5.4, the S_{Id}/I_D^2 upswing at high I_D is bigger for the BC device than for the TC one, which has a lower contact resistance than its BC counterpart (cf. Table 5.1).[5, 8, 25]

The contact resistances in TC and BC devices have been extracted using the transmission-line method (TLM)[25, 26] and was found to vary with V_G following an empirical expression $R_{sd}(V_G)=R_{sd0}(V_G-V_0)^{-\beta}$, where R_{sd0}, V_0 and β are fitting parameters.[25] A calculation involving a contact resistance contribution in Eq. 5.25, with a variable $R_{sd}(V_G)$ and S_{Rsd}/R_{sd}^2 treated as a constant parameter (see Table 1) enabled us to account reasonably well for the S_{Id}/I_D^2 leveling at high I_D (solid lines in Fig. 5.4), here $R_{sd0}=2.5\times10^9\Omega$ and $1.2\times10^{10}\Omega$, $V_0=-6$V and -8V, $\beta=4.4$ and 3.5, for the TC and BC OFET in Fig. 5.4, respectively. Larger R_{sd0} and smaller β are obtained in BC OFET than in TC one, as expected.[27, 28] The use of a constant $R_{sd}(V_G)$ would result in an exaggerated S_{Id}/I_D^2 upswing at high I_D as is shown in Fig. 5.4 (dash-dot curve), emphasizing the influence of $R_{sd}(V_G)$ on the LFN characteristics.

■ Scaling analysis

We also addressed another important feature of the transistor noise data, namely their dependence on the gate surface area, $W\times L$. From Eqs 5.23 and 5.24, it follows that S_{Id}/I_D^2 should be inversely proportional to $W\times L$. It was checked for both TC and BC devices with various L values (50, 100, 150μm) and W=500μm. As seen in Figs. 5.5(a) and 5.6(a), the intrinsic noise level S_{Id}/I_D^2 is inversely proportional to L, as expected. The $S_{Id}/I_D^2\times(WL)$ data are displayed in Figs. 5.5(b) and 5.6(b) as a function of the channel current density $I_D\times(L/W)$. The formation of universal curves both for the TC (Fig. 5.5b) and BC (Fig. 5.6b) devices confirms the gate surface area scaling. This implies a uniform surface distribution of LF noise sources underneath the whole device gate area. Note that the LFN data do not merge well in the region where the contact noise dominates, as they are independent of the channel (gate) dimensions. For the same reason, the dispersion of LFN data for BC devices is more pronounced in the high I_D limit.

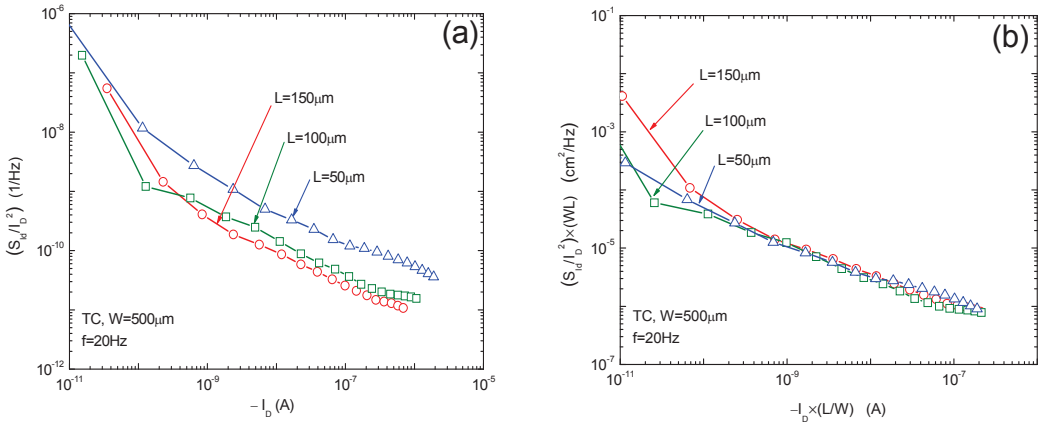


Figure 5.5 | Scaling effect. Before normalization (a), the S_{Id}/I_D^2 versus I_D for three TC OFETs, one can see that the noise level is inversely proportional to the gate area. After normalization (b), the normalized PSD $S_{Id}/I_D^2\times(WL)$ plotted *versus* drain current density $I_D\times(L/W)$ is shown to follow a universal dependence. Dispersion occurs at low and high current density. The former is due to system noise, and the latter is due to the contact resistance contribution. They are not scalable with the channel area.

It should also be noted that the dispersion of gate area scaling at high gate voltages or high current intensities, where the contact noise plays a major role as discussed above, implies negligible correlated mobility fluctuations. This is due to the fact that the correlation of mobility fluctuations should also lead to a good gate area scaling (cf. Eq. 5.20), which is clearly not observed in our case. This argument confirms the validity of Eq. 5.23 for this study and the contact contribution at high current intensities.

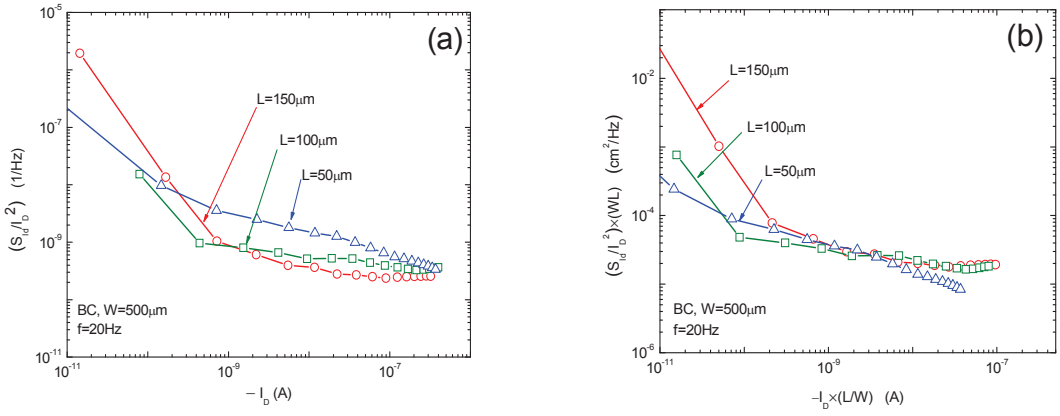


Figure 5.6 | The process of Fig. 5.5 applied to three BC OFETs. One can observe similar results as in TC OFETs. A larger dispersion arises from the normalized curves in Fig. 4(b) at high current density compared to TC OFETs. This is due to greater contact resistance in BC devices.

TABLE 5.1 Summary of the parameters` extracted from LFN data at f=20Hz and from static data for several TC and three BC pentacene OFETs.

Transistors	W(μm)	L(μm)	C_i(F/cm²)	R_{sd}(Ω.cm)	N_{SS}(1/eVcm²)	N_{ST}(1/eVcm²)	S_{Rsd}/R_{sd}^2(1/Hz)
TC1	500	150	7.1×10^{-8}±7%	3070±45%	6.0×10^{12}±50%	3.7×10^{12}±19%	1.7×10^{-7}±52%
TC2	500	100	8.1×10^{-8}±13%	3294±6%	3.2×10^{12}±41%	2.5×10^{12}±42%	1.1×10^{-7}±31%
TC3	500	50	11×10^{-8}±12%	3146±12%	5.0×10^{12}±48%	2.8×10^{12}±47%	5.5×10^{-8}±32%
BC1	500	150	4×10^{-8}±45%	78000±33%	1.0×10^{12}±62%	1.9×10^{13}±62%	4.9×10^{-8}±69%
BC2	500	100	4×10^{-8}±48%	110000±11%	1.2×10^{12}±69%	2.5×10^{13}±148%	1.3×10^{-8}±30%
BC3	500	50	4.4×10^{-8}±3%	96000±24%	9.2×10^{11}±25%	1.9×10^{13}±26%	3.0×10^{-8}±36%

The variations are the relative standard deviation from the average value calculated from several transistors for each group. The average value of R_{sd} is used for the next S_{Rsd}/R_{sd}^2 analysis.

5.2.5 Conclusions

In conclusion, we found that $1/f$ noise dominates in the LF noise in the studied pentacene OFETs. The S_{Id}/I_D^2 is found to vary as $(g_m/I_D)^2$ over several decades of I_D intensity, indicating the generation of carrier number fluctuations induced by trapping/detrapping process on the trap states distributed at top and bottom pentacene interfaces and/or in its crystalline bulk. The effective surface trap density is obtained around 2×10^{12}/eVcm² and 2×10^{13}/eVcm², for the TC and BC OFETs, respectively. The higher trap density in BC OFETs indicates more defects residing in the vicinity of contacts, leading to an equivalent higher surface trap density. Furthermore, the slow trap density extracted from LFN data is found to be close to the surface states density deduced from $I_D(V_G)$ sub-threshold slope, implying that the same defects are involved in the LF noise generation and charge trapping. In contrast, the Hooge mobility fluctuation model cannot account for the observed LFN behavior.

Secondly, we have shown that, at high I_D intensities, the contact resistance contribution dominates the OFETs LF noise and is responsible for the S_{Id}/I_D^2 leveling observed in the pentacene devices studied in this work. The higher contact resistance in BC devices results in a

higher upswing of S_{Id}/I_D^2. All of them are well explained by the additional fluctuations associated to a gate-voltage dependent contact resistance.

Finally, the good gate area scaling confirms the validity of carrier number fluctuations model, negligible correlated mobility fluctuations, and the predominant contact resistance contribution to the overall LF noise at high current intensities.

5.3 EXTRACTION OF CONTACT NOISE *(based on the paper published in Applied Physics Letters, 97, 033503, 2010)*[29]

The contact resistance in organic field-effect transistors (OFETs) has been intensively studied in the past years. It affects not only the static current-voltage (I-V) characteristics,[7] but also the low-frequency noise (LFN) properties.[9, 10, 12] Indeed, LFN measurements are well known to be a useful tool to investigate the channel transport and dielectric quality in terms of defect density. Many studies have reported that conventional LFN analyses could also be applied to organic transistors.[9-14, 19] However, the additional fluctuations from contact resistance usually dominate the overall LFN in OFETs at strong current intensities.[4, 9, 20] Therefore, conventional channel LFN studies become complicated since these parasitic contact fluctuations should be well extracted and separated from the overall measured LFN. In contrast to the evaluation of DC contact resistance, there is not to date any method to explicitly determine the power spectral density (PSD) of contact resistance fluctuations, S_{Rsd}, for LFN analysis in OFETs. Moreover, the gate-voltage dependence of contact resistance in such devices renders this issue more difficult.[8, 26, 27, 30] At present, the transfer-line method (TLM) is widely used for OFETs contact resistance evaluation.[8, 26, 31, 32] The total resistance incorporating channel and contact components of a set of OFETs with various channel dimensions varies linearly with channel length. The contact resistance can thus be extracted from the y-axis intercept of total resistance *versus* gate length plot. It is therefore possible to envisage that this procedure could also be employed to extract the power spectral density of contact resistance fluctuations, and thus obtaining the intrinsic channel LFN.

In this letter, we first introduce the issue of LFN study, in which the contact resistance fluctuations clearly dominate the measured LF noise. Next, we discuss the possible methodology based on TLM approach to extract the contact resistance PSD. Such a low-frequency noise transfer-line method (LFN TLM) is then applied to p-type and n-type OFETs.

Two types of OFETs are used for this study: vacuum evaporated pentacene OFETs (p-type, provided by NIMS) with bottom-contact (BC) and bottom-gate (BG) configuration,[4, 25] and solution-processed perylene diimide derivative OFETs (n-type, provided by CEA-Liten) with BC and top-gate (TG).[33] More information about device fabrication and noise measurement could be found in the given references.

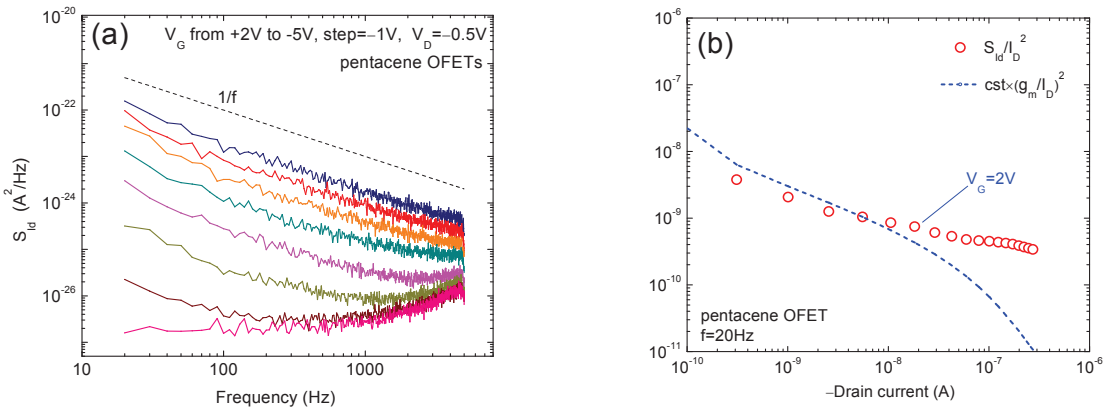


Figure 5.7 | (a) The measured LFN in a TC pentacene OFET, the dash line indicates the slope of $1/f$. (b) The superimposition of S_{Id}/I_D^2 and $constant \times (g_m/I_D)^2$ for this OFET. S_{Id}/I_D^2 begins to depart from $constant \times (g_m/I_D)^2$ at V_G=2V, implying the dominant fluctuations from contact resistance.

In Fig. 5.7(a), the PSD of drain current (I_D) fluctuations S_{Id} at various gate voltages exhibit pure $1/f$ spectrum at sufficiently high gate voltage or large drain current, for a pentacene OFET. The S_{Id} at f=20Hz normalized by drain current squared, S_{Id}/I_D^2, is plotted as a function of I_D in log-log scale, as shown in Fig. 5,7(b).[24] The carrier number fluctuations model has been shown to be well appropriate to account for such $1/f$ noise behavior (for more details see ref.[4]). S_{Id}/I_D^2 departs from the trend of the transconductance (g_m) to drain current ratio squared, $(g_m/I_d)^2$, at strong current intensities due to additional fluctuations from contact resistance which dominate the overall LFN.[4, 24]

As in the conventional TLM where total resistance is $R_{total}=R_{channel}+R_{sd}$, in LFN analysis, the PSD of total resistance fluctuations in *linear regime* reads $S_{Rtotal}=S_{Rchannel}+S_{Rsd}$, where $S_{Rchannel}$ and S_{Rsd} are the PSD of channel resistance and contact resistance fluctuations, respectively. So, we have:

$$S_{R_{total}} = \frac{S_{R_{channel}}}{R_{channel}^{\ 2}} \times R_{channel}^{\ 2} + \frac{S_{R_{sd}}}{R_{sd}^{\ 2}} \times R_{sd}^{\ 2} \tag{5.26}$$

where $S_{Rchannel}/R_{channel}^2$ and S_{Rsd}/R_{sd}^2 are the normalized PSD of channel and contact resistance fluctuations, respectively. $S_{Rchannel}/R_{channel}^2$ characterizes the intrinsic LFN in the channel, so for carrier number fluctuations, it could be represented by:[24]

$$S_{R_{total}} = \frac{q^2 kTN_{ST}}{WLC_i^{\ 2} f}\left(\frac{g_m}{I_D}\right)^2 \times R_{channel}^{\ 2} + \frac{S_{R_{sd}}}{R_{sd}^{\ 2}} \times R_{sd}^{\ 2} \tag{5.27}$$

where q is the electron charge, kT is the thermal energy, N_{ST} is the surface trap density(/eVcm^2), C_i is the unit area capacitance of the dielectric(F/cm^2). W and L are channel width and channel length, respectively. f is the frequency under study.

Similarly, if the Hooge mobility fluctuations are dominant, Eq. 5.26 reads:[24]

$$S_{R_{total}} = \frac{\alpha_H}{WLn_s f} \times R_{channel}^{\ 2} + \frac{S_{R_{sd}}}{R_{sd}^{\ 2}} \times R_{sd}^{\ 2} \tag{5.28}$$

where n_s is the surface carrier density and α_H is the Hooge parameter.

So, whatever the LF noise model, $S_{Rchannel}/R_{channel}^2$ scales as $1/WL$ and $R_{channel}$ varies as (L/W). S_{Rsd}/R_{sd}^2 characterizes the intrinsic contact resistance noise level, and it varies as $1/W$. Moreover, since $R_{sd}=\rho_{sd}/W$, where ρ_{sd} is the specific contact resistance, one can find that $S_{Rsd}\sim 1/W^3$.

Since, in linear regime, $S_{Rtotal}/R_{total}^2 = S_{Id}/I_D^2$ and $R_{total}=V_D/I_D$, Eqs 5.27 and 5.28 could also be expressed as:

$$S_{R_{total}} = \left(\frac{S_{I_d}}{I_D^{\ 2}}\right)\left(\frac{V_D}{I_D}\right)^2 = K\frac{L}{W^3} + \frac{S_{R_{sd}}}{R_{sd}^{\ 2}} \times R_{sd}^{\ 2} \tag{5.29}$$

where K is a constant, which comprises the contribution of $S_{Rchannel}$ for a given frequency.

At first glance, one can conclude from Eq. 5.29 that, by analogy to the conventional TLM (C-TLM), S_{Rsd} could be evaluated from the y-axis intercept of S_{Rtotal} *versus* L plots, for each gate bias. We name this method as C-LFN TLM. In principle C-LFN TLM should be applicable, however, due to huge parameter variations existing in OFETs, i.e. device-to-device scattering of constant K, this method is not reliable enough to extract S_{Rsd} from y-axis intercept. Similar discussion has been done in our work about $R_{sd}\times W$ evaluation,[33] in which a modified TLM (M-TLM) has been proposed. The M-TLM provides much more stable and reliable $R_{sd}\times W$ than that obtained by C-TLM.

Therefore, following the M-TLM approach, we divide both sides of Eq. 5.29 by L. We name this method as M-LFN TLM. If the channel widths of studied devices are different, S_{Rsd} should also be normalized by W. A specific contact PSD, $S_{Rsd}\times W^3$, is thus extracted instead of S_{Rsd}, which is proportional to ρ_{sd}^2 and independent of L and W. Hence its variations from device to device are expectedly very small like the $R_{sd}\times W$ in static TLM. The final equation used for the LFN M-TLM at a given frequency is therefore:

$$S_{R_{total}}\frac{W^3}{L}=\left(\frac{S_{I_d}}{I_D{}^2}\right)\left(\frac{V_D}{I_D}\right)^2\times\frac{W^3}{L}=K+(S_{R_{sd}}\times W^3)\frac{1}{L} \tag{5.30}$$

$S_{Rsd}\times W^3$ can be evaluated directly from the slopes of $S_{Rtotal}\times(W^3/L)$ *versus* $1/L$ plots. Indeed, the linear regression giving the slope *versus* $1/L$ minimizes the impact of K parameter scattering and maximizes the influence of small L, i.e. large $1/L$ values where the contact resistance noise contribution plays a major role.[33]

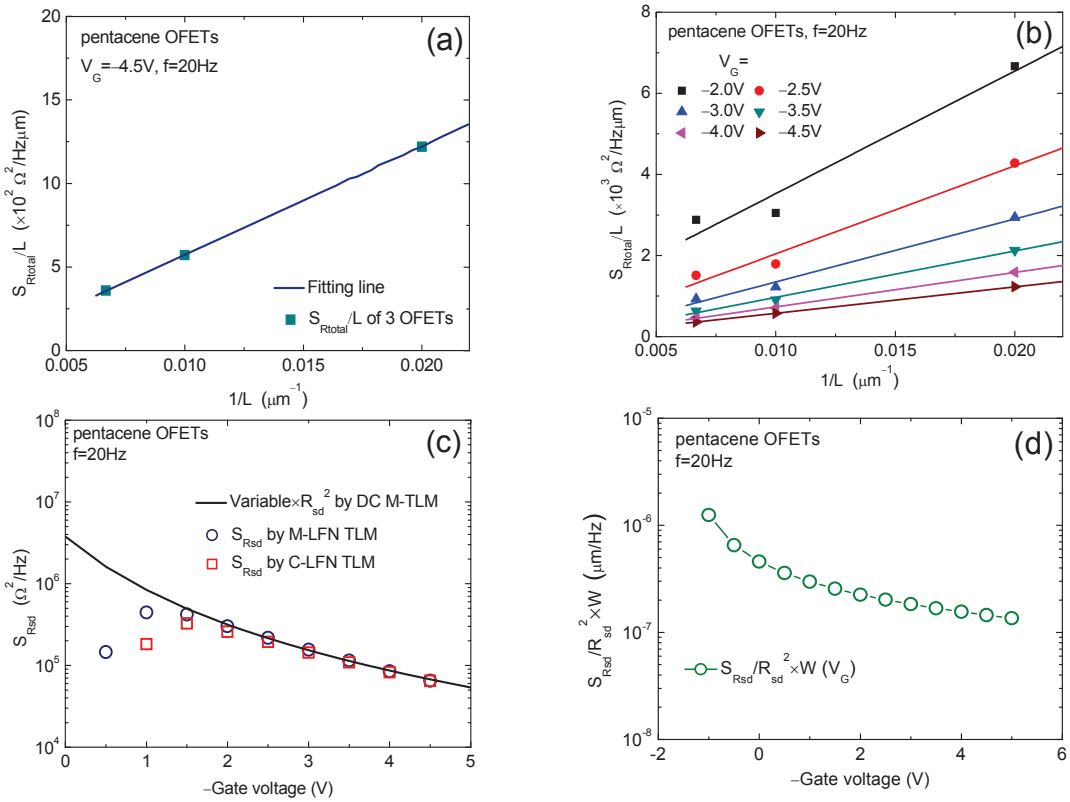


Figure 5.8 | (a) The L divided spectral density of total contact resistance fluctuations with respect to $1/L$, at V_G=–4.5V, for three pentacene OFETs (uniform W). S_{Rsd} could be extracted from the slope of the fitting line. (b) Complete plots of M-LFN TLM at various gate voltages, for the three OFETs. (c) The S_{Rsd} extracted by C-LFN TLM and M-LFN TLM. The black solid line indicates the superposition with the R_{sd} by static TLM, where the variable represents $S_{Rsd}/R_{sd}{}^2$, as shown in (d).

Figure 5.8(a) illustrates a plot of Eq. 5.30 at V_G=−4.5V, for three pentacene OFETs with L=50, 100 and 150μm and W=500μm. Because W is constant, it is not necessary to normalize the data here. The three OFETs exhibit good linearity, and complete plots from M-LFN TLM are shown in Fig. 5.8(b). Only the plots at V_G from −2V to −4.5V are showed for clarity as well as scattered data points obtained at small gate voltages. S_{Rsd} is evaluated from the slopes, and compared with the values obtained from the roughly applicable C-LFN TLM, as shown in Fig. 5.8(c). We can readily see that the two curves are very close, but the S_{Rsd} data from C-LFN TLM are disrupted at certain gate voltages due to wrong (negative) extrapolated values. Hence they cannot be displayed correctly in logarithmic scale. At the same time we can observe that S_{Rsd}, which mainly varies as $R_{sd}{}^2$, decreases very quickly with V_G because of the gate-voltage dependence of contact resistance $R_{sd}(V_G)$.

Furthermore, the S_{Rsd} extracted from M-LFN TLM is normalized by the $R_{sd}(V_G)$ evaluated by DC M-TLM, as shown by the solid curve in Fig. 5.8(c), here $R_{sd}(V_G)=4.5\times10^6[-V_G-(1.4)]^{-1}\Omega$cm.[25, 33] $S_{Rsd}/R_{sd}{}^2$ is found to decrease with V_G rather than being constant, as seen in Fig. 5.8(d), suggesting that the LFN level stemming from slow states defects in the contact region is related to the field effect and/or carrier concentration modulation. This phenomenon is probably similar to the gate voltage and/or carrier

concentration dependence occurring in contact transport region, leading to gate-voltage dependent contact resistance, particularly in TC OFETs.[26, 27] Here we have $S_{Rsd}/R_{sd}^2=1.2\times10^{-9}[-V_G-(1.4)]^{-0.8}$1/Hz or $(S_{Rsd}/R_{sd}^2)\times W=6\times10^{-7}[-V_G-(1.4)]^{-0.8}$ μm/Hz.

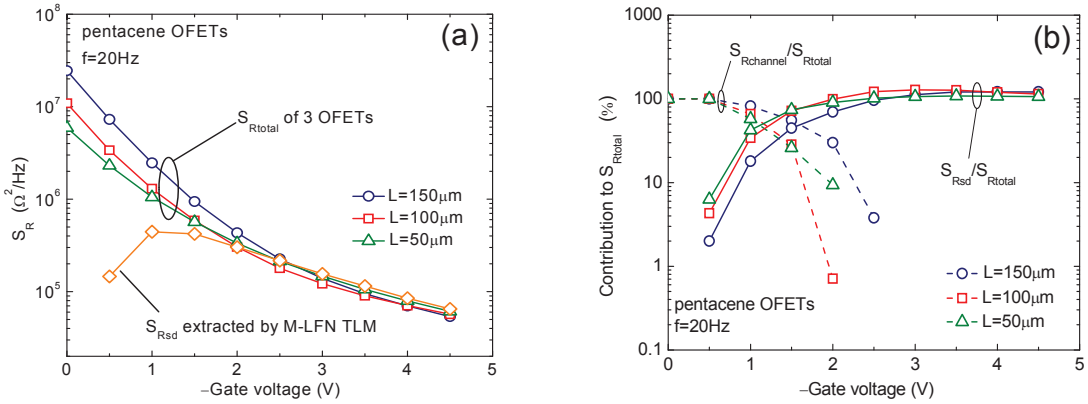
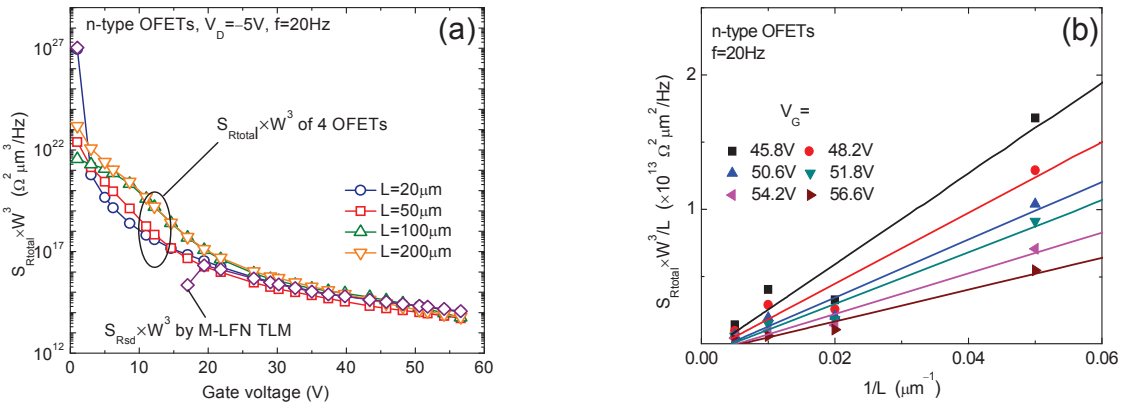


Figure 5.9 | (a) S_{Rtotal} of three pentacene OFETs with different L, and the extracted S_{Rsd}. The S_{Rtotal} of the three OFETs converge toward the extracted S_{Rsd} at high gate voltages. (b) Relative channel and contact contribution to the total LFN S_{Rtotal} in the three OFETs.

It should be noted that, in Fig. 5.8(b), $S_{Rtotal}\times(W^3/L)$ *vs* $1/L$ plots show better linearity at higher gate voltages. As can be seen from Fig. 5.7(b), this is due to the contribution of contact resistance noise, which dominates the overall LFN at $-V_G>2$V even below threshold voltage (V_T=1.5V) in the pentacene OFET, as further illustrated in Fig. 5.9(a). Hence the total PSD S_{Rtotal} of the three OFETs converge toward the contact resistance PSD S_{Rsd} at high gate voltages. That's why better linearity *vs* $1/L$ appears in this region. It should also be noted that the S_{Rsd} domination would be more pronounced in OFETs having smaller channel length, worse contact resistance, higher mobility or lower channel noise, since the fluctuations from contact resistance would become relatively more significant than those from transistor channel, analogously to the contact resistance effect on DC I-V characteristics.

With the extracted S_{Rsd}, the intrinsic channel LFN could be obtained by a direct subtraction $S_{Rchannel}=S_{Rtotal}-S_{Rsd}$. Such a contact resistance-free LFN could be used for the conventional LFN study. The channel and contact relative contributions to the total LFN are shown in Fig. 5.9(b). It is clear that, as the gate voltage is increased, the contact contribution completely dominates the overall LFN, with a more pronounced effect in short channel OFET, emphasizing the strong impact of contact resistance on OFETs LFN.

Finally, the same extraction procedure has been applied to n-type OFETs. The contact resistance contribution is also found completely dominating the overall LFN at strong current intensities like in pentacene OFETs, as shown in Fig. 5.10(a). The M-LFN TLM is plotted in Fig. 5.10(b), $S_{Rsd}\times W^3$ and normalized $(S_{Rsd}/R_{sd}^2)\times W$ are shown in Fig. 5.10(c) and Fig. 5.10(d), respectively. Here $R_{sd}(V_G)\times W=1.3\times10^8[V_G-(17.8)]^{-1.4}\Omega$.cm, and $(S_{Rsd}/R_{sd}^2)\times W\approx2\times10^{-6}$ μm/Hz. Note that the latter is nearly constant, with amplitude slightly higher than that in pentacene OFETs.



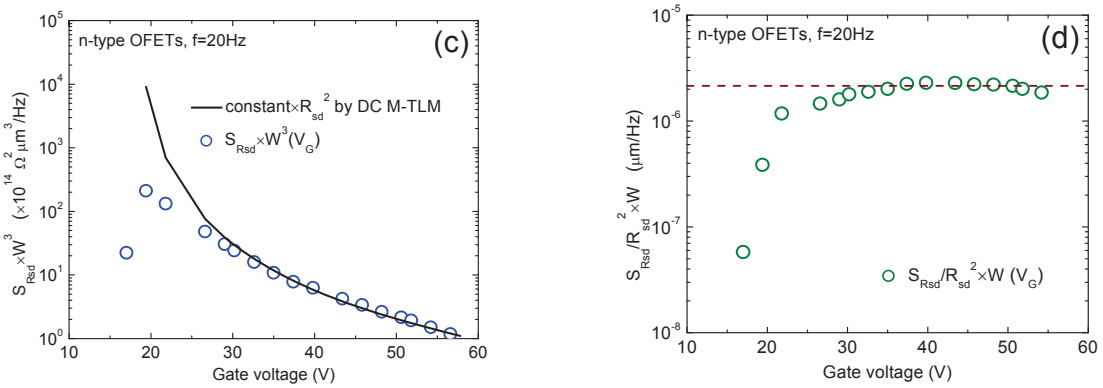


Figure 5.10 | The comparison of S_{Rtotal} of four n-type OFETs (various W) with the extracted S_{Rsd}, the completely dominant S_{Rsd} could be identified at high gate voltages. (b) Complete plots of M-LFN TLM for S_{Rsd} extraction. (c)The extracted S_{Rsd} in the set of n-type OFETs, and it could also be well normalized by the R_{sd}×W obtained by static TLM. The constant (S_{Rsd}/R_{sd}^2)×W is obtained, as shown in figure (d).

It worth mentioning that, if the thickness of the organic semiconductor is significantly different, the comparison of $(S_{Rsd}/R_{sd}^2)\times W$ would be meaningless, particularly in staggered OFETs. In our case, the thicknesses of pentacene and n-type organic semiconductor are both around 50nm. Otherwise, a fair comparison of contact resistance PSD should be done after normalizing S_{Rsd}/R_{sd}^2 by the organic semiconductor film thickness. This is due to the fact that the LF noise originating from access region might, in general, be inversely proportional to the contact region volume.

In summary, TLM has been extended to evaluate the power spectral density of contact resistance fluctuations, S_{Rsd}, in linear regime, whatever the channel $1/f$ noise sources. $S_{Rsd}\times W^3$ has been demonstrated to be directly and accurately extracted from the slopes of $(S_{Id}/I_D^2)\times(V_D/I_D)^2\times W^3/L$ *versus* $1/L$ plots, for each gate bias. The gate-voltage dependent $S_{Rsd}(V_G)\times W^3$ has then been normalized by the gate-voltage dependent $R_{sd}(V_G)\times W$ extracted by DC M-TLM. Gate bias dependent and nearly constant $(S_{Rsd}/R_{sd}^2)\times W$ behaviors have been found in pentacene and n-type OFETs, respectively. Therefore, such a modified LFN TLM technique enables to explicitly investigate the origin and location of low-frequency noise sources in organic transistors.

5.4 DISGNOSIS OF CONTACT NOISE SOURCES *(based on the paper published in Applied Physics Letters, 98, 033505, 2011)*[34]

Contact resistance nowadays is a crucial subject in organic field-effect transistors (OFETs) due to its strong impact not only on dc characteristics[7] but also on low-frequency noise (LFN) properties.[9, 10, 12] LFN measurements are well known as an elegant tool to investigate the carrier transport at the interface and the dielectric defects in standard devices,[17] and it has also been applied to OFETs.[9-12, 14, 19] On the other hand, because of the additional fluctuations from contact resistance which completely dominate the overall LFN at strong current intensity,[9, 12] the conventional LFN analysis based on the channel noise becomes ambiguous. In our previous work, the contact LF noise was extracted by a modified LFN transmission-line method (TLM), independently of the channel noise sources.[29] This method offers the possibility to distinguish which one of the two classical LFN models is dominant in contact noise, as it is done for the conventional channel LFN analysis.[4, 17] In this letter, the contact noise is first extracted, and then, a diagnostic procedure for identifying the contact noise sources is proposed.

Two types of staggered OFETs (the source/drain contacts and the gate dielectric are on the opposite side of organic film, contrasting to the coplanar OFETs in which the contacts and the gate dielectric are on the same side) were used for this study: solution-based printing

bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) OFETs with bottom-contact and top-gate configuration (provided by CEA-Liten)[35] and vacuum evaporated pentacene OFETs with top-contact and bottom-gate configuration (provided by NIMS).[25] More information about device fabrication and noise measurement can be found in the given references.

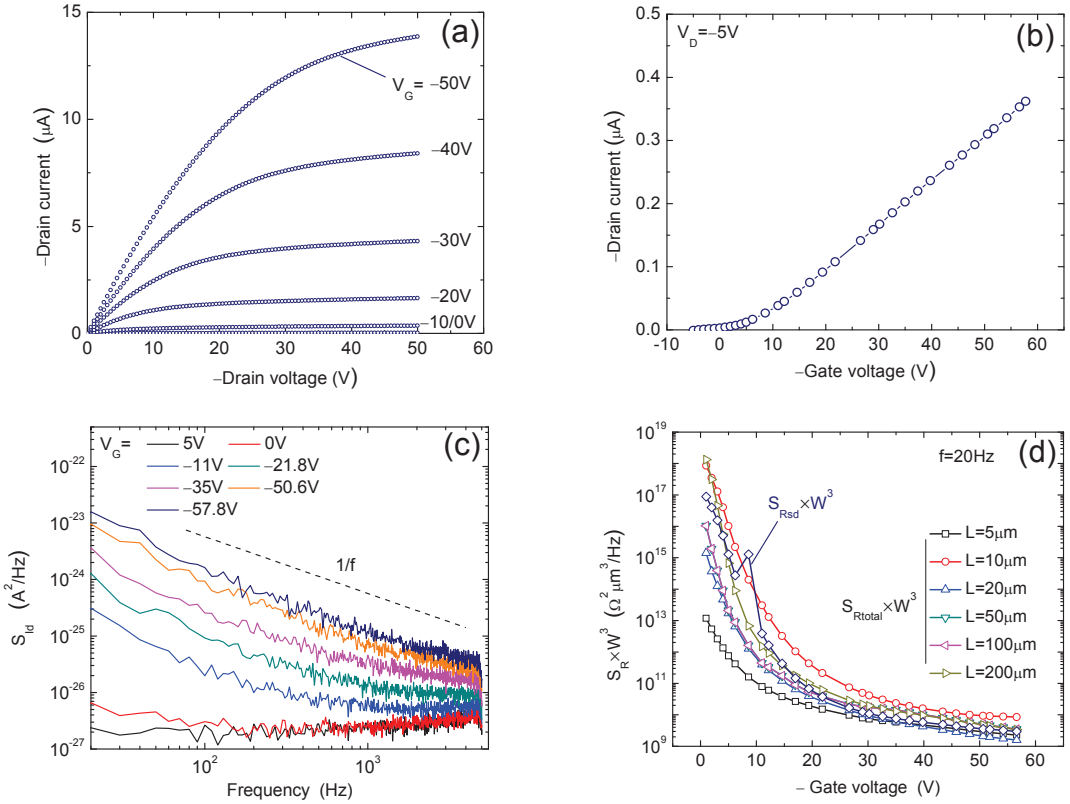


Figure 5.11 | (a) and (b) are output and transfer characteristics at V_D=−5V measured LFN in a TIPS-pentacene OFET (W=200μm, L=50μm), respectively. (c) LFN measured in this OFET, the dash line indicates the slope of 1/f. (d) PSD of total resistance fluctuations at 20Hz, for a set of OFETs with different channel length, and the open diamond represents the extracted contact noise.

The output and transfer characteristics of a TIPS-pentacene OFET are shown in Figs. 5.11(a) and 5.11(b), respectively. During the DC measurements at various gate voltages (V_G), the drain current (I_D) fluctuations are recorded, as shown in Fig. 5.11(c), and their power spectrum densities (PSD) S_{Id} clearly show a 1/f-type spectrum. The S_{Id} at a fixed frequency (here at f=20Hz) is normalized by drain current squared, S_{Id}/I_D^2, and it is plotted with respect to the drain current in log-log scale.[17] Two classical LFN models are concerned, i.e., carrier number and Hooge mobility fluctuations models. As the gate voltage or the drain current is increased, the additional fluctuations from contact resistance dominate the overall LF noise.[9, 12, 24, 29] The diagnosis of the channel LFN sources has been treated elsewhere,[4] here we focus on the contact noise sources.

As discussed in our previous work,[29] the PSD of total resistance fluctuations S_{Rtotal}, at a fixed frequency, in *linear regime* can be obtained from the measured S_{Id} as:

$$S_{R_{total}}\frac{W^3}{L}=\left(\frac{S_{I_d}}{I_D{}^2}\right)\left(\frac{V_D}{I_D}\right)^2\times\frac{W^3}{L}=K+(S_{R_{sd}}\times W^3)\frac{1}{L} \tag{5.31}$$

where W and L are the channel width and length, respectively, K is a constant which comprises the channel noise contribution, S_{Rsd} is the PSD of contact resistance fluctuations, and R_{sd} is the contact resistance. Hence, S_{Rsd}/R_{sd}^2 is the normalized PSD of contact resistance fluctuations which characterizes the intrinsic contact LF noise.

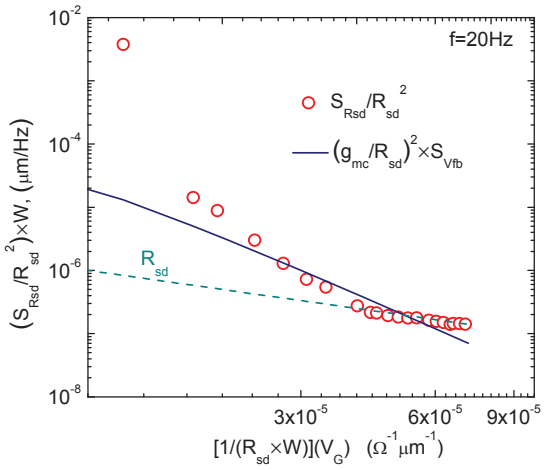


Figure 5.12 | Normalized PSD of contact LF noise in the above set of TIPS-pentacene OFETs, is shown by open circles. The solid line represents the tendency of $(g_{mc}/R_{sd})^2$, for the carrier number fluctuations model. The dash line indicates the slope of R_{sd}, predicted by the Hooge mobility fluctuations model.

The $S_{Rtotal}\times W^3$ of six OFETs with various L are shown in Fig. 5.11(d), and the W normalized contact resistance PSD $S_{sd}\times W^3$ is then extracted according to Eq. 5.31.[29] The contact resistance was evaluated previously by dc modified-TLM,[33] here $R_{sd}(V_G)\times W = 1.7\times 10^5[-V_G-(5.5)]^{-0.63}$ Ωcm. The PSD of intrinsic contact noise $(S_{Rsd}/R_{sd}^2)\times W$ is plotted against $1/R_{sd}$ in Fig. 5.12 and will be used for further analysis.

In the case of channel carrier number fluctuations (Δn) scheme,[15] the charge carriers are captured/released by the slow traps in gate dielectric. This dynamic trapping/detrapping process induces a fluctuation of flat-band voltage via the relation $\delta V_{fb}=-\delta Q_{it}/(WLC_i)$, where δQ_{it} is the fluctuation of interface trapped charges,[16] C_i is the unit area capacitance of gate dielectric (F/cm^2). δV_{fb} causes a drain current fluctuation given by $\delta I_d=-g_m\delta V_{fb}$, if the effective mobility fluctuation $\delta\mu_{eff}$ is negligible,[17] with g_m being the transconductance. Hence one obtains $S_{Id}/I_D^2=(g_m/I_d)^2S_{Vfb}$, in which S_{Vfb} is the PSD of the flat-band voltage fluctuations. If the charge trapping is due to a tunneling process, hence $S_{Vfb}=q^2kTN_{ST}/(WLC_i^2f)$ where N_{ST} is the surface trap density (eV^{-1}cm^{-2}).[17]

For contact noise, the free carriers must cross the contacts and thus are captured/released by the slow traps in the gate dielectric of the contact region, leading to a fluctuation of contact resistance. Since R_{sd} is gate-voltage dependent, the δV_{fb} analogously causes a fluctuation of contact resistance δR_{sd}. Defining the parameter $g_{mc}=dR_{sd}/dV_G$, the normalized contact resistance noise becomes $S_{Rsd}/R_{sd}^2=(g_{mc}/R_{sd})^2S_{Vfb}$. Finally, the carrier number fluctuations expression for *one contact* LF noise reads:

$$\frac{S_{R_{sd}}}{R_{sd}^{\ 2}}=\left(\frac{g_{mc}}{R_{sd}}\right)^2\times\frac{q^2kTN_{STC}}{2W_CL_CC_i^{\ 2}f} \tag{5.32}$$

where q is the electron charge, kT is the thermal energy, N_{STC} is the equivalent surface trap density in contact region (eV^{-1}cm^{-2}), W_C and L_C are the contact width and length, respectively, and f is the frequency under study.

In the case of Hooge mobility fluctuations ($\Delta\mu$) scheme,[18] the charge carriers undergo a scattering process, resulting in a fluctuation of carrier mobility. The noise level is inversely proportional to the total carrier number in the device $S_{Id}/I_D^2=\alpha_H/(WLn_sf)$, where n_s is the surface carrier density and α_H is the Hooge parameter. The latter reveals the noise amplitude in the channel and thus the carrier scattering intensity.

Hence for *contact noise*, that expression becomes $S_{Rsd}/R_{sd}^2=\alpha_H/(2W_CL_Ct_{SC}nf)$ where n is the volume carrier density in contact region and t_{SC} is the organic film thickness. Given the equivalent length of contact volume $L_C/2$,[27] the contact resistance reads $R_{sd}=2t_{SC}/(nq\mu W_CL_C)$ for predominant vertical carrier transports, here μ is the carrier mobility, assumed to be equal to the OFETs' low-field mobility.[25] So we have:

$$\frac{S_{R_{sd}}}{R_{sd}^{\ 2}}=\frac{\alpha_Hq\mu R_{sd}}{4t_{SC}^{\ 2}f} \tag{5.33}$$

Using Eqs. 5.32 and 5.33, one can discriminate the contact LF noise sources. Indeed, since $I=V/R$ (V is constant), S_{Rsd}/R_{sd}^2 is thus plotted against $1/R_{sd}$ in log-log scale. If $S_{Rsd}/R_{sd}^2(1/R_{sd})$

varies following the tendency of $(g_{mc}/R_{sd})^2$, one can conclude that the carrier number fluctuations dominate the contact LF noise sources. On the other hand, if $S_{Rsd}/R_{sd}^2(1/R_{sd})$ decreases as R_{sd} (cf. Eq. 5.33), it indicates that the Hooge mobility fluctuations prevail.

The $S_{Rsd}/R_{sd}^2(1/R_{sd})$ of TIPS-pentacene OFETs is shown in Fig. 5.12. These OFETs have the same L_C=100μm and t_{SC}=100nm, with C_i=1.48×10^{-9} F/cm^2. Since W_C=W and as it varies in the different studied OFETs, S_{Rsd}/R_{sd}^2 is thus normalized by W, namely $(S_{Rsd}/R_{sd}^2)\times W$. From this figure one can see that $S_{Rsd}/R_{sd}^2\times W(1/R_{sd})$ can be well superimposed to the variation of $(g_{mc}/R_{sd})^2$, indicating that carrier number fluctuations prevail. The equivalent surface trap density is extracted as N_{STC}=6.6×10^{13}/eVcm^2. Note that this value is one thousand times higher than that previously extracted in the channel (N_{ST}=10^9-10^{10}/eVcm^2) by conventional LFN analysis, implying much more defects distributed in the contacts. If one assumes that the traps are evenly distributed in the whole organic film depth, this areal density should correspond to a volume trap concentration of 6.6×10^{18}/eVcm^3. This result is not surprising since the deposition of organic material over the contacts in these bottom-contact (BC) devices results in a large number of traps around the contacts. It should be noted that, for those BC devices, the channel trap density has been found higher than in top-contact (TC) devices,[4] and it is therefore significantly raised in the contacts. In addition, the vertical transport may also be responsible for such a high N_{STC}. Meanwhile one can observe a clear deviation at high gate bias, however it can be well interpreted by the $\Delta\mu$ model which predicts $S_{Rsd}/R_{sd}^2(1/R_{sd})\sim R_{sd}$, as illustrated by the dashed line. With the previously evaluated mobility μ= 2 cm^2/Vs, the Hooge parameter is found to be ≈1, which is comparable with the reported values for the channel LFN.[9, 12, 13] From all the results, one could conclude that the two models might coexist, i.e., the Δn model dominates at small gate bias whereas the $\Delta\mu$ model prevails at high gate bias.

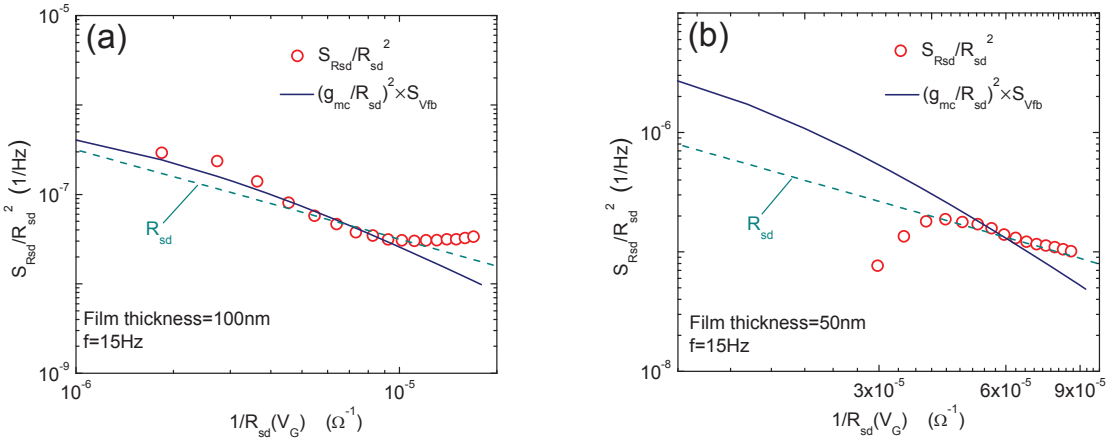


Figure 5.13 | Diagnosis process of Fig. 2 applied to a set of pentacene OFETs having the pentacene film thickness of 100nm (a) and 50nm (b), respectively.

The same process is applied to two sets of pentacene OFETs having different film thickness: 50nm and 100nm with uniform W_C=W=1000μm, L_C=125μm and C_i=7.98×10^{-8} F/cm^2. We examine first the OFETs with t_{SC}=100nm, as shown in Fig. 5.13(a). $S_{Rsd}/R_{sd}^2(1/R_{sd})$ can be roughly superimposed to the $(g_{mc}/R_{sd})^2$ variation, where a N_{STC}=1.8×10^{17}/eVcm^2 is derived with $R_{sd}(V_G)$=6×10^5[$-V_G$−(−1.1)]$^{-1.05}$ Ω. Such a so high N_{STC} is not physically realistic since exceeding the molecular areal density, hence the Δn model cannot explain the contact noise in these transistors. On the other hand, it seems that the $\Delta\mu$ model should be applicable. From Eq. 5.33, one can extract α_H≈0.5 using the evaluated μ=0.1 cm^2/Vs. This α_H is a little smaller than α_H=5 reported by Necliudov *et al.* in TC pentacene OFETs,[9] but it is feasible since considerable progress in material preparation, surface treatment and fabrication technology have been made during this period. Note that α_H=0.5 obtained here is for the contact LF noise and that α_H=5 is for the channel LF noise.[9] Moreover, one can find that S_{Rsd}/R_{sd}^2 departs from R_{sd} variation at

high gate bias, implying another LFN source which cannot be accounted for by such formulations of Δn or $\Delta\mu$ models.

Next we analyze the OFETs of t_{SC}=50nm, as shown in Fig. 5.23(b). Because the contact resistance and the contact noise exhibit slight gate-voltage dependences, the spanning range of $1/R_{sd}$ is very narrow so that the diagnosis becomes ambiguous, here $R_{sd}(V_G)=7.1\times10^4[-V_G-(-2.05)]^{-0.8}$ Ω. The accordance of the Δn model is not clear and the correspondingly derived $N_{STC}=3.6\times10^{18}$/eVcm^2 is too high to reach a reasonable interpretation. However the $\Delta\mu$ fits very well in the measurable range, where one obtains α_H=3 (with μ=0.1 cm^2/Vs), which is 6 times higher than in their counterparts with t_{SC}=100nm, in agreement with the trend reported in ref.[13]

In summary, a contact LF noise diagnostic procedure has been presented. Once the normalized contact noise S_{Rsd}/R_{sd}^2 depends on the gate voltage, the $S_{Rsd}/R_{sd}^2(1/R_{sd})$ in log-log scale could be used for diagnosis. If it follows the tendency of $(g_{mc}/R_{sd})^2$, one can say that the carrier number fluctuations dominate. If it varies as R_{sd} from small to high gate voltage, one can assert that the Hooge mobility fluctuations are prevailing. In our TIPS-pentacene OFETs, the extracted contact LFN is well explained by the Δn model as well as the $\Delta\mu$ model. The former dominates the small biasing region, in which a 1000 times higher trap density than that in the channel is obtained, implying much more process-induced defects in contacts. The latter dominates the high biasing region, where a Hooge parameter of about 1 is derived. For the pentacene OFETs, the contact LFN is well interpreted by the $\Delta\mu$ model, whereas the Δn model gives unrealistic trap density. As the thickness of pentacene film is decreased, the Hooge parameter increases from 0.5 to 3 for the OFETs of 100nm and 50nm thick pentacene film, respectively. Therefore, this method proved very suitable to identify the LF noise sources in the contact resistance of organic transistors.

5.5 LFN IN OTHER OFETS

■ PTAA OFETs (IZM)

At the beginning of this thesis, I studied several PTAA OFETs made by IZM (Germany). As seen in Fig. 5.14, the measured LF noise of the drain current clearly shows a $1/f$ type spectrum and the noise level increases with the gate voltage or the drain current. The normalized S_{Id}/I_D^2 is shown in Fig. 5.15. The concurrently measured drain current versus gate voltage is shown in Fig. 5.16, thus the $(g_m/I_D)^2$ against drain current is obtained, as seen in Fig. 5.17.

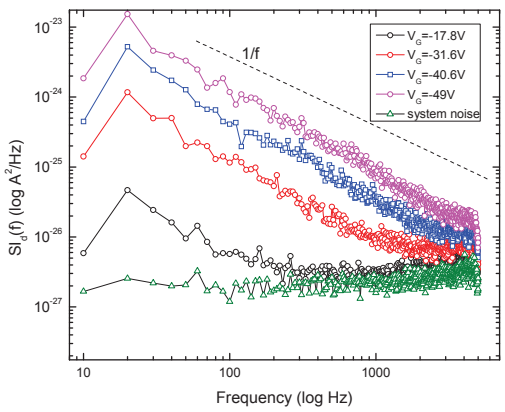


Figure 5.14 | The PSD of the drain current fluctuations versus frequency in log-log scale. The dashed line indicates the slope of 1/f. The green triangles represent the maximum system noise, i.e. measured at zero drain voltage and at maximum gate voltage. It's clear that the system noise is much lower than the effective noise, hence it could be disregarded.

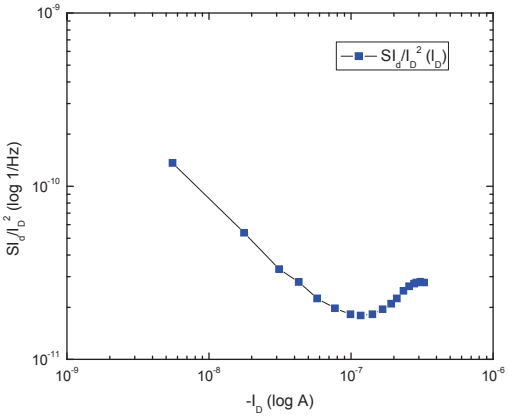


Figure 5.15 | The normalized PSD of the drain current fluctuations versus drain current in log-log scale.

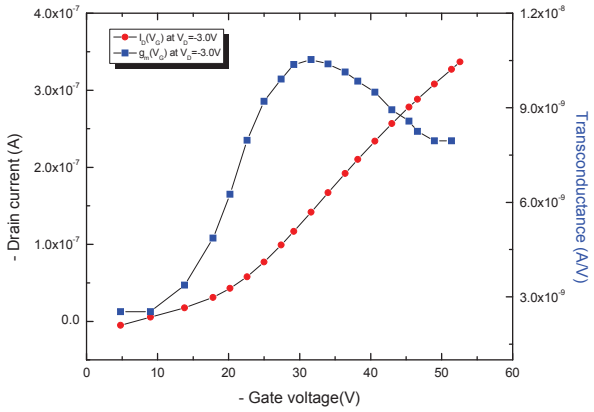


Figure 5.16 | The measured static transfer characteristics at V_D=-3V, the calculated transconductance is represented by the blue squares.

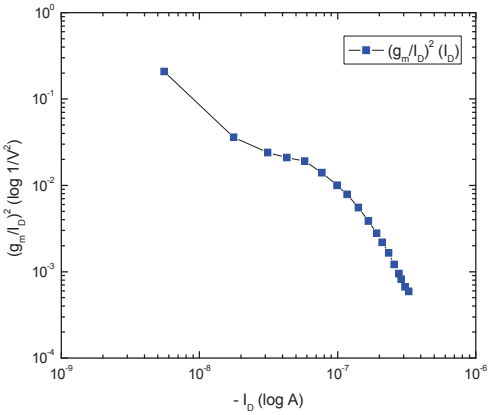


Figure 5.17 | The transconductance normalized by the drain current squared versus drain current in log-log scale.

It's clear that the noise data of S_{Id}/I_D^2 doesn't decrease with I_D following I_D^{-1}, which is predicted by the Hooge mobility fluctuations model. On the other hand, the S_{Id}/I_D^2 could be well superimposed with $(g_m/I_D)^2\times$constant as the drain current is small than 10^{-7}A , where the constant corresponds to a volume trap density around 5×10^{18}/eVcm^3. If the same tunnel attenuation distance 0.1nm can be applied, one will obtain an equivalent surface trap density 5×10^{10}/eVcm^2, and this value is reasonable for organic transistors since it is around ten times higher than that in classical silicon MOSFETs. Hence, one can say that the carrier number fluctuations model is responsible for the observed $1/f$ noise. Note the deviation arising from the two curves' superposition at stronger current intensity, as discussed above this is due to the additional fluctuations originated from the contact resistance. According to Eq. 5.25, the $(g_m/I_D)^2\times$constant supplemented with $S_{Rsd}(I_D/V_D)^2$ represented by green squares could well fit the experimentally measured noise data, where the $S_{Rsd}/R_{sd}^2=1.6\times10^{-9}$/Hz with the Y function method extracted $R_{sd}=5.2\times10^6\Omega$ or $R_{sd}\times W=3.1\times10^7\Omega$cm. Here the gate-voltage dependent contact resistance is not necessary to explain the contact noise.

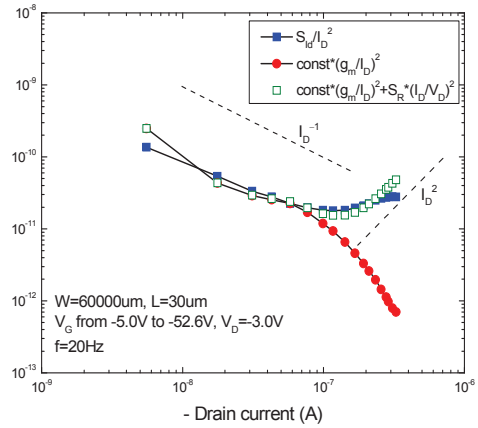


Figure 5.18 | Superposition of SI_d/I_D^2 and $(g_m/I_D)^2$xconstant. The two dashed lines indicate the slope of I_D^{-1} and I_D^2. The green squares represent the $(g_m/I_D)^2$ x constant supplemented with the additional fluctuations coming from contact resistance.

■ PTAA OFETs (CEA-LITEN)

I studied several sets of PTAA OFETs made by CEA-LITEN, the given codes are 379, 383, 404 and 727. Compared to the counterparts made in IZM, these PTAA OFETs show also clear $1/f$ noise, thus the same process stated above can be applied here. For simplicity, only the different results are shown and the extracted parameters are summaried in Table 5.2.

As seen in Fig. 5.19, the S_{Id}/I_D^2 doesn't decrease with I_D following I_D^{-1} but could be well superimposed with $(g_m/I_D)^2\times$constant, corresponding to an equivalent trap density of $N_{ST}=5.6\times10^{15}$/eVcm^2. Thus the carrier number

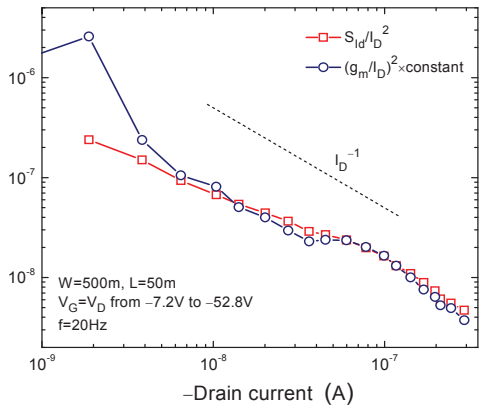


Figure 5.19 | Diagnosis of LFN sources in LITEN PTAA OFETs, code 379, location L2C1.

fluctuations model also accounts for the $1/f$ noise measured in these LITEN PTAA OFETs. Note that the obtained trap density is so high, five orders of magnitude higher than their IZM counterparts, implying the poor quality. However, with the considerable progress made in the next generations, this trap density is significantly decreased, e.g. 379→404→727, see Table 5.2. One should also note that the contact noise doesn't affect the overall LFN at strong current intensities, this might be due to the poor quality and the low mobility, resuting in smaller drain current. On the other hand, it might be due to the relatively smaller contact resistance and its contribution to the overall LFN (higher channel noise in LITEN PTAA OFETs on substrate 379, 404) is smaller than in the IZM transistors.

Owing to the availality of different channel dimensions, i.e. W and L, we performed also a scaling analysis. As shown in Fig. 5.20a, before channel dimension normalization, the intrinsic noise level (S_{Id}/I_D^2) is inversely proportional to the channel surface, i.e., the higher intrinsic noise level is observed in small channel surface device, as expected. After normalization, namey $S_{Id}/I_D^2 \times (WL)$ data are plotted as a function of the channel current density $I_D \times (L/W)$, as seen in Fig. 5.20b. It's clear that a universal curve is obtained. We cannot at this stage provide a more precise description of noise generation mechanism, but one can still identify that because of the $1/f$ noise, the scaling law and the corresponding carrier number fluctuation model, the LFN sources are uniformly distributed near the dielectric/semiconductor interface. The trap densities here are much higher than that in the conventional silicon MOSFETs where the N_{ST} is around the order of the magnitude of 10^9/eVcm^2, and also higher than that in RIKEN pentacene OFETs ($N_{ST}=10^{12}$/eVcm^2).

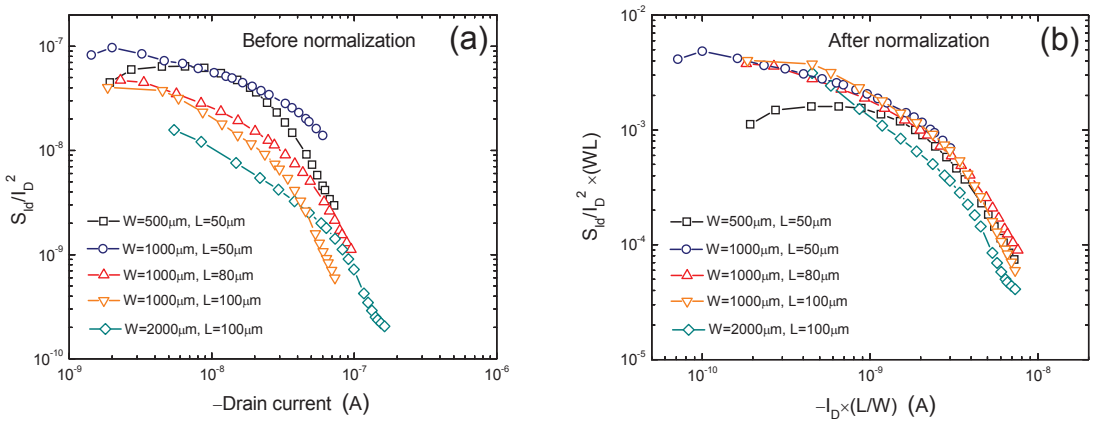


Figure 5.20 | Scaling analyses for a set of PTAA OFETs (code 379). Before channel dimension normalization (a), the intrinsic noise level decreases with the channel surface. After normalization(b), an universal curve is obtained.

■ N-type OFETs (CEA-LITEN)

We studied also a set of n-type OFETs made by CEA-LITEN with N-type semiconductor N1400, code 729. Fig. 5.21 shows the LFN sources diagnosis for a n-type transistor. The normalized noise data (S_{Id}/I_D^2) doesn't decrease with the drain current with I_D^{-1}, indicating that the Hooge mobility fluctuations model is not involved. On the other hand, S_{Id}/I_D^2 could be well fitted by the $(g_m/I_D)^2$ with an adjusting constant, which corresponds to an equivalent surface trap density $N_{ST}=6\times10^{11}$/eVcm^2. At higher current intensity, the noise often fast increases with drain current (not shown here), as observed in pentacene

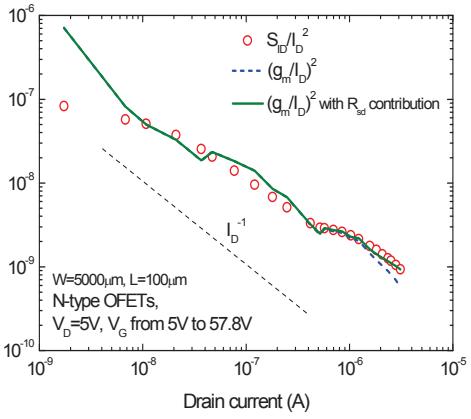


Figure 5.21 | Diagnosis of LFN sources in a n-type OFET, code 729, location C7.

OFETs(RIKEN) and PTAA OFETs(IZM). This is due to the additional contact noise which dominates the overall LFN at high current intensities. But here the upswing is not obvious, implying the gate-voltage dependent contact resistance effect, hence the empicial expresssion $R_{sd}=R_{sd0}(V_G-V_0)^{-\beta}$ is also used, where the R_{sd0}, V_0 and β are fitting parameters. Here $R_{sd0}=8\times10^6\Omega$, $V_0=10$V, $\beta=1$, which is exactly equal to the value obtained by TLM extraction. [36] More detailed information on the contact noise has been discussed above.

■ TIPS-pentacene (CEA-LITEN)

A set of high performance TIPS-pentacene OFETs made by CEA-LITEN were also examined for their LFN sources. As shown in Fig. 5.22, it's clear the Hooge mobility flucutations model cannot be applied however the two curves of (S_{Id}/I_D^2) and $(g_m/I_D)^2\times$constant versus I_D could be well superimposed, implying the carrier number fluctuations model is concerned. The corresponding surface trap density is found to be $N_{ST}=5\times10^{10}$/eVcm^2 in this OFET, this N_{ST} value sometimes is as low as 10^9/eVcm^2, comparable to that in classical silicon MOSFETs. Also, the additional flucutuatinos from contact resistance are responsible for the measured overall LFN level upswing at high current intensities because of the ultra low channel noise level. Hence the relative impact of contact noise becomes significant at high current intensities. More detailed information on the contact noise has been discussed above.

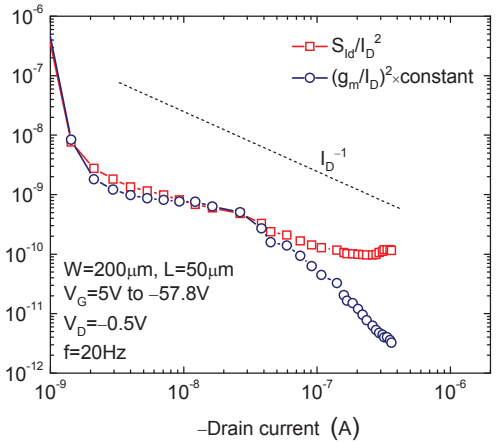


Figure 5.22 | Diagnosis of LFN sources in a TIPS-pentacene OFET, code 715, location T5.

5.6 CONCLUSIONS

In this chapter, we addressed the low-frequency noise in organic transistors. First, the basic noise theory and analysis methods were presented. And then, we investigated the low-frequency noise in pentacene OFETs. It was found that the carrier number fluctuation model is concerned, and the obtained surface trap density is higher in bottom-contact devices relative to top-contact transistors. With comparing the surface states deduced from the subthreshold slope technique, one found that the surface traps densities are comparable to the surface states densities in top-contact OFETs, whereas in bottom-contact counterparts the surface traps densities are much higher than the surface states densities, whose values remain the same level with respect to the top-contact transistors. So the same (surface) states might be involved in the noise and the sub-threshold transport, and the increased surface traps density in bottom-contact devices is due to the process induced defects around the contacts, which is also responsible for the low mobility and higher contact resistance by DC characterizations. Meanwhile, one observed a clear contact noise at high current intensities, particularly in bottom-contact OFETs. This contact noise is well explained by superposition of channel noise and contact noise with using a gate-voltage dependent contact resistance, a constant contact resistance would result in too drastic increase of contact noise. The good channel area scaling indicates that the noise sources are uniformly distributed over the channel area, in the dielectric, in the organic bulk or at the organic/dielectric interface.

Next, we developed a contact noise extraction method by extending the DC TLM to noise analysis. This method is successfully applied into our two sets of OFETs. A gate-voltage dependent intrinsic contact noise (denoted by normalized contact noise PSD) is found in top-contact and bottom-gate pentacene OFETs and this might be due to the gate-voltage dependent carrier transport in the contact region, especially in these staggered devices. We also analyzed the contact noise impact on the overall noise for different channel length OFETs, it was found that the contact noise is more important in short-channel devices, similarly to the DC contact resistance impacts on the I-V characteristics. Finally, a nearly constant contact noise is obtained in n-type OFETs.

With the extracted contact noise, we developed a diagnostic process for staggered OFETs, as it is done for the channel noise sources diagnosis. Both the carrier number fluctuations model and the Hooge mobility fluctuations model are involved in the contact noise of TIPS-pentacene OFETs (top-gate and bottom-contact), and the former dominates the low-current region and the latter prevails the high-current region. But only the latter is involved in the contact noise of pentacene OFETs, and the Hooge parameter increases with decreasing the pentacene film thickness, reflecting higher scattering intensity in thinner film.

Table 5.2. Summary of the parameters extracted by DC data and LFN data in some of studied OFETs

Transistor					DC data				LFN data		
OSC	code	W (μm)	L (μm)	C_i (F/cm^2)	μ (cm^2 V^{-1}s^{-1})	V_T (V)	R_{sd} (Ωcm)	N_{SS} (eV^{-1}cm^{-2})	$\Delta n/\Delta\mu$	N_{ST} (eV^{-1}cm^{-2})	Note
Pentacene-RIKEN	TC1	500	150	7.5×10^{-8}	0.43	−2.1	2800	5.8×10^{12}	Δn	2.8×10^{12} (*L*)	
Pentacene-RIKEN	TC2	500	100	9.3×10^{-8}	0.34	−1.6	3100	6.2×10^{12}	Δn	2.0×10^{12} (*L*)	
Pentacene-RIKEN	TC3	500	50	9.5×10^{-8}	0.36	0.7	3400	4.3×10^{12}	Δn	1.6×10^{12} (*L*)	
Pentacene-RIKEN	BC1	500	150	4.9×10^{-8}	0.12	0.7	5.6×10^{4}	1.1×10^{12}	Δn	8.7×10^{12} (*L*)	
Pentacene-RIKEN	BC2	500	100	4.7×10^{-8}	0.07	2.3	1.1×10^{5}	1.9×10^{12}	Δn	5.8×10^{12} (*L*)	
Pentacene-RIKEN	BC3	500	50	4.5×10^{-8}	0.04	0.8	1.6×10^{5}	0.8×10^{12}	Δn	1.5×10^{12} (*L*)	
Pentacene-NIMS	50nm	1000	60	8×10^{-8}(t)	0.16	0.03	NA	1.1×10^{13}	Δn	2.4×10^{12} (*L*)	Tsc=50nm
Pentacene-NIMS	50nm	1000	80	1.8×10^{-7}	0.15	−0.3	NA	1×10^{13}	Δn	3.2×10^{12} (*L*)	Tsc=50nm
Pentacene-NIMS	50nm	1000	100	1.4×10^{-7}	0.17	−0.25	NA	1.1×10^{13}	Δn	4×10^{12} (*L*)	Tsc=50nm
Pentacene-NIMS	50nm	1000	120	8×10^{-8}(t)	0.2	−0.18	NA	1.1×10^{13}	Δn	4.8×10^{12} (*L*)	Tsc=50nm
Pentacene-NIMS	100nm	1000	60	2.4×10^{-7}	0.07	−1	NA	8.1×10^{12}	Δn	9×10^{12} (*L*)	Tsc=100nm
Pentacene-NIMS	100nm	1000	80	2×10^{-7}	0.1	−0.9	NA	7.7×10^{12}	Δn	1.2×10^{13} (*L*)	Tsc=100nm
Pentacene-NIMS	100nm	1000	100	8×10^{-8}(t)	0.1	0.06	NA	1×10^{13}	Δn	8.8×10^{12} (*L*)	Tsc=100nm
Pentacene-NIMS	100nm	1000	120	1.5×10^{-7}	0.09	−1.3	NA	8.7×10^{12}	Δn	2×10^{13} (*L*)	Tsc=100nm
PTAA-IZM	30-D8	6×10^{4}	30	1.3×10^{-9}	6.6×10^{-4}	−16.7	1.1×10^{7}	4.3×10^{10}	Δn	5.2×10^{10} (*L*)	
PTAA-IZM	20-D4	4×10^{4}	20	1.5×10^{-9}	7.1×10^{-4}	−14	4×10^{6}	1.6×10^{12}	Δn	3.1×10^{12} (*L*)	
PTAA-IZM	16-D3	3.2×10^{4}	16	1.4×10^{-9}	5.4×10^{-4}	−18	7.5×10^{6}	2.3×10^{10}	Δn	4.9×10^{12} (*L*)	
PTAA-LITEN	379-l2c1	500	50	2.4×10^{-8}	0.9×10^{-3}	−9.2	5.4×10^{6}	NA	Δn	3.8×10^{15} (*L*)	5.6×10^{15} (*S*)
PTAA-LITEN	379-l3c4	1000	50	3.6×10^{-8}	0.7×10^{-3}	−9	4.7×10^{6}	NA	Δn	1.6×10^{16} (*L*)	8.5×10^{15} (*S*)
PTAA-LITEN	379-l5c5	1000	80	1.9×10^{-8}	1.9×10^{-3}	−9	4.4×10^{6}	NA	Δn	4.4×10^{16} (*L*)	1.5×10^{16} (*S*)
PTAA-LITEN	379-l3c2	1000	80	1.8×10^{-8}	1.6×10^{-3}	−8.8	3.7×10^{6}	NA	Δn	9.4×10^{15} (*L*)	1.3×10^{16} (*S*)
PTAA-LITEN	379-l3c3	1000	100	1.6×10^{-8}	2.8×10^{-3}	−11	4.1×10^{6}	NA	Δn	1.2×10^{16} (*L*)	5.5×10^{15} (*S*)
PTAA-LITEN	379-l4c6	2000	100	1.2×10^{-8}	3.7×10^{-3}	−8.3	4.5×10^{6}	NA	Δn	4.7×10^{16} (*L*)	8.7×10^{15} (*S*)
PTAA-LITEN	404-l4c1	500	50	2.7×10^{-8}	0.9×10^{-3}	−19.7	2.8×10^{6}	NA	Δn	2.8×10^{15} (*L*)	
PTAA-LITEN	404-l1c5	1000	50	1.8×10^{-8}	1.8×10^{-3}	−19.3	4.1×10^{6}	NA	Δn	5.1×10^{15} (*L*)	1.2×10^{15} (*S*)
PTAA-LITEN	404-l2c3	2000	50	1.6×10^{-8}	2.4×10^{-3}	−15	2.9×10^{6}	NA	Δn	2.7×10^{14} (*L*)	
PTAA-LITEN	404-l1c2	1000	80	1.1×10^{-8}	3.8×10^{-3}	−17	4.8×10^{6}	NA	Δn	3.2×10^{15} (*L*)	4.6×10^{13} (*S*)
PTAA-LITEN	404-l3c3	1000	100	0.9×10^{-8}	1.3×10^{-3}	−19.5	7.6×10^{6}	NA	Δn	1.3×10^{15} (*L*)	
PTAA-LITEN	404-l2c4	2000	100	0.8×10^{-8}	5.7×10^{-3}	−14.3	3.4×10^{6}	NA	Δn	1.4×10^{14} (*L*)	
PTAA-LITEN	727-R14	2000	5	1.48×10^{-9}(t)	0.01	−8.5	1.9×10^{5}	3.7×10^{11}	Δn	8.6×10^{10} (*L*)	
PTAA-LITEN	727-R15	2000	10	1.48×10^{-9}(t)	0.016	−8.1	2×10^{5}	3.6×10^{11}	Δn	1.9×10^{11} (*L*)	
PTAA-LITEN	727-T14	600	20	1.48×10^{-9}(t)	0.026	−9.4	1.5×10^{5}	2.5×10^{11}	Δn	1.9×10^{11} (*L*)	
PTAA-LITEN	727-S13	2000	50	1.48×10^{-9}(t)	0.034	−7.5	2.2×10^{5}	2.2×10^{10}	Δn	5.2×10^{10} (*L*)	

PTAA-LITEN	727-R6	1000	100	1.48×10^{-9}(t)	0.033	–7.2	2.6×10^{5}	6.4×10^{10}	Δn	5.9×10^{10} (*L*)
PTAA-LITEN	727-T13	1000	50	1.48×10^{-9}(t)	0.035	–9.1	1.2×10^{5}	2.5×10^{10}	Δn	5.5×10^{10} (*L*)
N1400	729-A3	10000	20	1.48×10^{-9}(t)	0.02	14.8	NA	4.9×10^{11}	Δn	7.6×10^{12} (*L*)
N1400	729-B14	200	50	1.48×10^{-9}(t)	0.35	39	1.8×10^{4}	4.7×10^{10}	Δn	2.8×10^{11} (*L*)
N1400	729-C7	5000	100	1.48×10^{-9}(t)	0.28	41	NA	6.7×10^{10}	Δn	5.9×10^{11} (*L*)
N1400	729-D13	1000	20	1.48×10^{-9}(t)	0.12	40	5.9×10^{4}	1.8×10^{10}	Δn	2.2×10^{11} (*L*)
N1400	729-E13	1000	50	1.48×10^{-9}(t)	0.25	40.5	5.9×10^{4}	5.3×10^{10}	Δn	2.1×10^{11} (*L*)
N1400	729-E14	600	20	1.48×10^{-9}(t)	0.15	37.5	5.9×10^{4}	6.3×10^{10}	Δn	2.1×10^{11} (*L*)
TIPS-pentacene	715-T4	2000	100	1.48×10^{-9}(t)	2.8	–15	3.5×10^{3}	7.2×10^{11}	Δn	2.8×10^{11} (*L*)
TIPS-pentacene	715-T5	200	50	1.48×10^{-9}(t)	2.7	–9.5	2.8×10^{3}	9.9×10^{11}	Δn	5.1×10^{10} (*L*)
TIPS-pentacene	715-T11	2000	200	1.48×10^{-9}(t)	3.5	–13.3	5×10^{3}	7.3×10^{11}	Δn	5.4×10^{10} (*L*)
TIPS-pentacene	715-T14	600	20	1.48×10^{-9}(t)	1.8	–12.2	3.5×10^{3}	7.4×10^{11}	Δn	5.9×10^{9} (*L*)
TIPS-pentacene	715-R14	2000	5	1.48×10^{-9}(t)	0.6	–0.6	3.4×10^{3}	8.3×10^{11}	Δn	6.4×10^{9} (*L*)
TIPS-pentacene	715-R15	2000	10	1.48×10^{-9}(t)	0.8	–10.8	3.9×10^{3}	7.3×10^{11}	Δn	4.3×10^{10} (*L*)

Here the mobility and the threshold voltage are extracted by Y function. For Ci, "t" represents the value calculated from the technological dielectric thickness and theoretical permittivity. For Nst, "L" and "S" represent the trap density extracted in linear regime and in saturation regime, respectively.

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Conclusions

In this three years Ph.D. thesis (October 2008-September 2011), I focused on the study of organic transistors, including DC characterizations, low-frequency noise measurements and modeling, DC characteristics modeling and carrier transport modeling. The expected objectives are accomplished.

In the first chapter of this thesis, I reviewed the principal issues related to organic semiconductors. The carrier transport in organic semiconductors in comparison with that in single-crystal silicon is firstly presented. The weak van der Waals forces interacting between molecules, the large band-gap, the disorders and the impurities give rise to a complex and low-efficiency carrier transport. Then we presented the principal parameters associating with the performances of organic semiconductors: mobility and conductivity. Next, one discussed the principal organic semiconductors: small molecular, polymeric and n-type semiconductors; the currently typical organic semiconductors are discussed. In the end, the other (organic) materials used for OFETs' fabrication are also analyzed: organic dielectrics, organic electrodes and interconnections, organic substrates as well as organic passivation layers.

In the second chapter, the attention was paid to the organic transistors. One first examined the OFETs' structures (configurations), OFETs apply a thin film of organic materials instead of the single-crystal bulk in silicon MOSFETs and thereby, OFETs are also often referred to as OTFTs. Because of the different location of gate and S/D electrodes, there are four configurations for OFETs fabrication and each configuration has their own advantages and disadvantages. Next, we discussed the OFETs' operating mechanism which is similar to the conventional MOSFETs. The only one difference is that the depletion/inversion of Si MOSFETs is absent in OFETs due to the intrinsic organic semiconductors and the thin film structure, the charge is injected from contacts into the organic film thus the OFETs operate directly in accumulation mode while a proper gate voltage is applied. We also analyzed the OFETs' principle parameters: mobility, threshold voltage, contact resistance, subthreshold slope etc. The relevant issues and critical results in the literature have also been addressed. Finally, we investigated the principal techniques for organic transistors fabrication.

In the third chapter, the efforts are devoted to the OFETs' DC characterizations. We first discussed the mostly used method in the community for the mobility and threshold voltage extraction by the transfer characteristics in saturation regime. It was found not very reliable and not powerful enough (e.g. for contact resistance extraction). And then we introduced the Y function method and it was proved to be a powerful method by applying into our pentacene OFETs. The field-effect mobility and the effective mobility are severely affected by the contact resistance, but the low-field mobility is free from such contact effects. Moreover, this Y function method can directly extract the contact resistance in individual transistors, not as the average value obtained by TLM, offering an investigation of contact resistance evolution in one transistor, which is important for the bias stress analysis. Afterwards, one addressed other methods for the principal parameters extraction, including our modified and power TLM. This modified TLM much improves the extraction reliability (with fewer channel lengths and at smaller gate voltages) and accuracy (smaller dispersion around the real value). The power TLM extends the contact resistance extraction from linear regime to saturation regime, enabling a full gate- and drain- voltage extraction; thus one can observe the contact resistance dependences on the external biases. In the end, we described the principal results of our studied OFETs in this thesis.

In the forth chapter, I concentrated on the modeling work. At first, a modeling of the OFETs' DC characteristics is presented. This model is based on a 1-D analytical solution of Poisson's equation for the organic film in organic transistors, by which the potential profile and

the carrier concentration in the organic film can be derived. Combing the Gauss law, one can calculate the charge per unit area in the organic film at each gate voltage, and thus obtaining the drain current in linear regime for an organic transistor. This model reveals the importance of the open surface on the overall carrier transport, the subthreshold transport in the film is a volume phenomenon rather than the widely believed superficial one also because of the intrinsic organic semiconductors; the band bending is only significant near the gate dielectric as a high gate voltage is applied. The calculated results well account for the measurement data of pentacene OFETs, however the bulk traps cause a large deviation in fitting to the experimental data of TIPS-pentacene OFETs. We thus performed simulations on traps, with different location (surface/bulk), different energy distribution of DOS and donor/acceptor-like, the analytical solution involving shallow bulk traps introduced from the open surface well explains the experimental data.

Next, we focused on the carrier transport in organic semiconductors and organic transistors. Three mobilities are extracted against temperature by different methods in our TIPS-pentacene OFETs, the low-field mobility exhibits the best reliability and its easy of use, particularly at low temperatures and for short-channel transistors. The analysis of OFETs having diverse channel lengths indicated that the overall carrier transport in short-channel OFETs (e.g. L=5μm) is nearly dominated by the transport in the contact vicinity, suggesting that a more intrinsic transport study in organic semiconductor is better carried out on the relatively longer-channel devices. The observed temperature dependences of mobility are well explained by a mobility model using Kubo-Greenwood integral. A constant diffusivity in the band would result in a high mobility decreasing with temperature, implying inherent band-like transport in delocalized states. A window-like diffusivity with two symmetric mobility edges would lead to a fully localized carrier transport at low carrier density and at low temperatures, the mobility decreases to zero. Increasing temperature activates the carrier distribution in the band and improves the hopping efficiency, manifesting a thermally activated mobility with large activation energies. A generic Gaussian-like diffusivity in the band gives a smooth transition of hopping transport to band-like transport from band tails to band center. It well explains the observed mobility variation with temperature in the long- and short- channel OFETs, in the latter the disorder level and defect density are higher. One also addressed the gate-voltage or carrier density dependent mobility, and found that it is due to the hopping transport. This impact is more pronounced in the disordered system and at lower temperatures.

Afterwards, we analyzed the carrier mobility in organic transistors with considering the charge distribution in the film. The simulation results indicated that the assumption of zero potential at free/open surface will give rise to a large deviation in the threshold voltage and subthreshold slope from the real situations, where the floating surface potential at free surface corresponds to a volume transport in subthreshold region. This impact is even getting greater in the OFETs with thinner organic film. Taking account of this effect, the whole conductivity in the organic film is calculated by using the Kubo-Greenwood integral, leading to the effective mobility for all carriers. This analysis enables a mobility study at each gate voltage, instead of the previous one by using the carrier density for a bulk of organic semiconductor. So the effective mobility is analyzed with respect to the gate voltage and temperature, for different delocalized-localized states hybridization level and various disorder levels.

In the last chapter, we addressed the low-frequency noise in organic transistors. First, the basic noise theory and analysis methods were presented. And then, we investigated the low-frequency noise in pentacene OFETs. It was found that the carrier number fluctuation model can be applied, and the obtained surface trap density is higher in bottom-contact devices relative to top-contact transistors. With comparing the surface states deduced from the subthreshold slope technique, one found that the surface traps densities are comparable to the surface states densities in top-contact OFETs, whereas in bottom-contact counterparts the surface traps densities are much higher than the surface states densities, whose values remain the same level with

respect to the top-contact transistors. So the same (surface) states might be involved in the noise and the subthreshold transport, and the increased surface traps density in bottom-contact devices is due to the process induced defects around the contacts, which is also responsible for the low mobility and higher contact resistance by DC characterizations. Meanwhile, one observed a clear contact noise at high current intensities, particularly in bottom-contact OFETs. This contact noise is well explained by superposition of channel noise and contact noise with using a gate-voltage dependent contact resistance, a constant contact resistance would result in too drastic increase of contact noise. The good channel area scaling indicates that the noise sources are uniformly distributed over the channel area, in the dielectrics, in the organic bulk or at the organic/dielectric interface.

Next, we developed a contact noise extraction method by extending the DC TLM to noise analysis. This method is successfully applied into our two sets of OFETs. A gate-voltage dependent intrinsic contact noise (denoted by normalized contact noise PSD) is found in top-contact and bottom-gate pentacene OFETs and this might be due to the gate-voltage dependent carrier transport in the contact region, especially in these staggered devices. We also analyzed the contact noise impact on the overall noise for different channel length OFETs, it was found that the contact noise is more important in short-channel devices, similarly to the DC contact resistance impacts on the I-V characteristics. Finally, a nearly constant contact noise is obtained in n-type OFETs.

With the extracted contact noise, we developed a diagnostic process for staggered OFETs, as it is done for the channel noise sources diagnosis. Both the carrier number fluctuations model and the Hooge mobility fluctuations model are involved in the contact noise of TIPS-pentacene OFETs (top-gate and bottom-contact), and the former dominates the low-current region and the latter prevails the high-current region. But only the latter is involved in the contact noise of pentacene OFETs, and the Hooge parameter increases with decreasing the pentacene film thickness, reflecting higher scattering intensity in thinner film.

Prospects

Even though a lot of interesting results and considerable progresses have been made in this thesis, there are still several issues left which need more detailed and deeper exploration in future studies.

With regard to the OFETs' DC characterizations and the relevant modeling, a crucial subject is the contact effects. One should clarify the origins of the contact resistance in different structure (charge injection barrier, interface dipole, charge injection area, bulk dominant resistance or low-conducting contact region), and next to address how the contacts affect the device performances (e.g., mobility, threshold voltage, contact resistance, stability).

With regard to the carrier transport study, there are a number of topics. Following the DC characteristics modeling in this thesis, the free surface plays an important role in subthreshold transport of organic transistors; one could investigate this effect by applying different biases on the free surface or by using double-gate OFETs. Another issue is the single-crystal OFETs, because they are free from structural disorder and thus are useful to observe the extrinsic influences, such as gate insulators and contacts. These high quality devices could also enable a study

of intrinsic carrier transport in organic semiconductors, which can be conducted by Hall-Effect measurements and other techniques.

With regard to the low-frequency noise study, the first subject is to clarify the origins of noise sources in different type of devices, e.g., polymer (amorphous), polycrystalline and single-crystal OFETs, or OFETs of different structures. A detailed modeling to reveal the formation of the observed $1/f$ noise by these origins can be subsequently carried out. LFN measurements (combining bias stress measurements) on single-crystal OFETs with various gate dielectrics are also interesting to investigate for the evolution of traps density, and thus the evolution of the defect density.

List of publications during thesis:

■ Journal papers:

1. Y. Xu,_T. Minari, K. Tsukagoshi, J. Chroboczek and G. Ghibaudo: 'Direct evaluation of low-field mobility and access resistance in pentacene field-effect transistors', *Journal of Applied Physics*, **107**, 11, pp.114507-7, June, 2010.

2, Y. Xu, T. Minari, K. Tsukagoshi, R. Gwoziecki, R. Coppard, F. Balestra, J. Chroboczek and G. Ghibaudo: 'Extraction of low-frequency noise in contact resistance of organic field-effect transistors', *Applied Physics Letters*, **97**, 3, pp.033503-3, July 2010.

3, Y. Xu, R. Gwoziecki, I. Chartier, R. Coppard, F. Balestra and G. Ghibaudo: 'Modified transmission-line method for contact resistance extraction in organic field-effect transistors', *Applied Physics Letters*, **97**, 6, pp.063302-3, August, 2010.

4, Y. Xu, R. Gwoziecki, R. Coppard, M. Benwadih, T. Minari, K. Tsukagoshi, J. Chroboczek, F. Balestra and G. Ghibaudo: 'Diagnosis of low-frequency noise sources in contact resistance of staggered organic transistors', *Applied Physics Letters*, **98**, 3, pp.033505-3, January, 2011.

5, Y. Xu, F. Balestra and G. Ghibaudo: 'Theoretical analysis of carrier mobility in organic field-effect transistors', *Applied Physics Letters*, **98**, pp.233302-3, June, 2011.

6. Y. Xu, T. Minari, K. Tsukagoshi, J. Chroboczek, F. Balestra and G. Ghibaudo: 'Origion of low-frequency noise in pentacene field-effect transistors', *Solid State Electronics*, **61**, 1, pp.106-110, July, 2011.

7, Y. Xu, T. Minari, K. Tsukagoshi, R. Gwoziecki, R. Coppard, M. Benwadih, J. Chroboczek, F. Balestra and G. Ghibaudo: 'Modeling of static electrical properties in organic field-effect transistors', *Journal of Applied Physics*, **110**, pp.014510-12, July, 2011.

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9, Y. Xu, M. Benwadih, R. Gwoziecki, R. Coppard, T. Minari, C. Liu, K. Tsukagoshi, J. Chroboczek, F. Balestra and G. Ghibaudo: 'Carrier mobility in organic field-effect transistors ', *Journal of Applied Physics*, **110**, pp.104513-9, November, 2011

■ Conference papers:

1. Y. Xu, T. Minari, K. Tsukagoshi, K. Bock, M. Fadlalah, G. Ghibaudo and J.A. Chroboczek : 'Study of Organic Material FETs by Combined Static and Noise Measurements', Oral presentation at *ICNF 2009*, Pisa, June 2009.

2. Y. Xu, G. Ghibaudo, F. Balestra, J.A. Chroboczek, R. Gwoziecki, I. Chartier and R. Coppard : 'Static and low frequency noise characterization of P-type polymer and N-type small molecule organic field-effect transistors', Oral presentation at *ICOE 2010*, Paris, June 2010.

3. Y. Xu, F. Balestra, J.A. Chroboczek, G. Ghibaudo, T. Minari, K. Tsukagoshi, R. Gwoziecki and R. Coppard : 'Analysis of Low-Frequency Noise in Organic Field-Effect Transistors Combing Static and Noise Data', Poster presentation at *ICNF 2011*, Toronto, June 2011.

4. Y. Xu, G. Ghibaudo, F. Balestra, M. Benwadih, R. Gwoziecki and R. Coppard : 'On the Temperature Dependence of Carrier Mobility in Organic Transistors', Oral presentation at *ICOE 2011*, Roma, June 2011.

Title: Characterization and modeling of static properties and low-frequency noise in organic field-effect transistors (OFETs)

Abstract: Organic transistors recently attract much attention because of their unique advantages over the conventional inorganic counterparts. However, the understanding of their operating mechanism and the carrier transport process are still very limited, this thesis is devoted to such a subject. Chapter 1 presents the organic semiconductors regarding carrier transport, parameters, typically applied materials. Chapter 2 describes the issues related to organic transistors: structure, operating mechanism, principal parameters and fabrication technologies. Chapter 3 deals with the static properties characterization. The commonly used methods are firstly presented and then the Y function method is introduced. Afterwards, the characterization methods for principles parameters are separately discussed. The experimental results on our organic transistors are finally described. Chapter 4 focuses on the modeling on the basis of the experimental data, regarding DC characteristics modeling with a solution for Poisson's equation, carrier mobility modeling with using Kubo-Greenwood integral as well as a theoretical analysis of OFETs' carrier mobility involving a solution of Poisson's equation. Chapter 5 analyzes the low-frequency noise in organic transistors. One firstly addresses the channel noise sources and then concentrates on the contact noise extraction and contact noise sources diagnosis. The noise measurements on other samples are also presented.

Key words: Characterization, modeling, simulation, low-frequency noise, organic field-effect transistors

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Titre: Caractérisation et modélisation des propretés électriques et du bruit à basse fréquence dans les transistors organiques à effet de champ (OFETs)

Résumé: Les transistors organiques attirent actuellement beaucoup d'attention en raison des avantages uniques par rapport à leur homologue inorganique. En revanche, la compréhension physique du fonctionnement et du transport des porteurs de charge est très limitée. L'objectif de cette thèse est de contribuer à apporter une meilleure compréhension des transistors organiques. Le Chapitre 1 présente les semi-conducteurs organiques : le mécanisme de conduction, les paramètres essentiels, les matériaux typiques etc. Le Chapitre 2 discute des transistors organiques en termes de structures, de mécanismes de fonctionnement, de paramètres principaux et des procédés de fabrication. Le Chapitre 3 étudie la caractérisation statique. Après les méthodes classiques, la méthode de la fonction Y est introduite. Subséquemment, des techniques pour extraire les paramètres principaux sont présentées séparément. Enfin, les résultats expérimentaux sur nos échantillons sont exposés. Sur la base des données mesurées, les travaux de modélisation sont présentés dans le chapitre 4. Premièrement, une solution de l'équation Poisson est introduite qui donne la distribution de potentiel et donc la distribution de porteurs dans le film organique. Avec la prise en compte des pièges, les résultats obtenus par simulation sont en bon accord avec les données expérimentales. A partir de mesures des caractéristiques de courant –tension effectuées à basse température, on propose une procédure d'analyse de la mobilité en utilisant l'intégrale de Kubo-Greenwood. Ensuite, prenant en compte la distribution de porteurs dans le film organique, une solution de l'équation de Poisson est donnée et la mobilité effective est calculée en fonction de la tension de grille et de la température. Le Chapitre 5 est consacré à l'analyse du bruit à basse fréquence. On étudie d'abord le bruit du canal où une domination du bruit provenant des contacts est observée. En conséquence, une méthode TLM pour l'extraction du bruit des contacts est présentée. Ensuite, un procédure d'analyse des sources de bruit dû au contact est aussi proposée. Les résultats de bruit obtenus sur des transistors organiques de différentes origines sont également discutés à la fin.

Mots clés: Caractérisation, modélisation, simulation, bruit à basse fréquence, transistors organiques